KSETA chip design course

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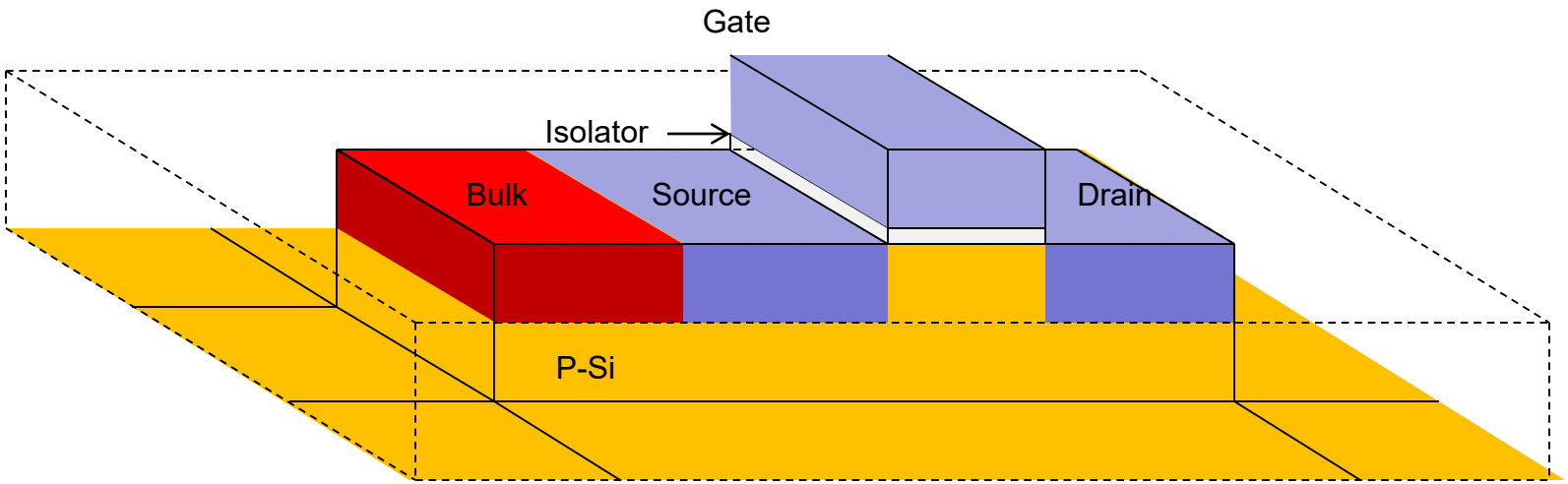
Literature

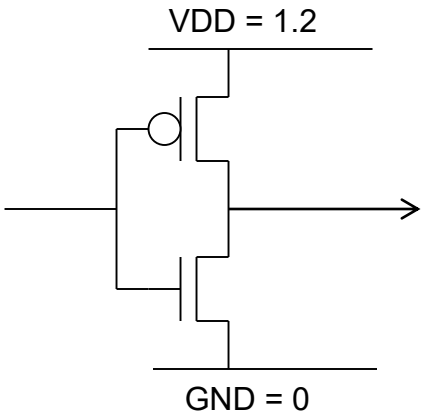
- Link to the lecture design of analogue circuits 2022/23
- https://ilias.studium.kit.edu/ilias.php?ref_id=1926247&cmd=view&cmdClass=ilrepositorygui&cmdNode=x1&baseClass=ilrepositorygui
- (Everyone can join the ILAS course)
- Link to older lectures (English/German)
- https://adl.ipe.kit.edu/english/28.php

Books about analog IC design

- Behzad Razavi:
- Design of Analog CMOS Integrated Circuits
- Fundamentals of Microelectronics
- RF Microelectronics
- Design of CMOS phase locked loops

Introduction

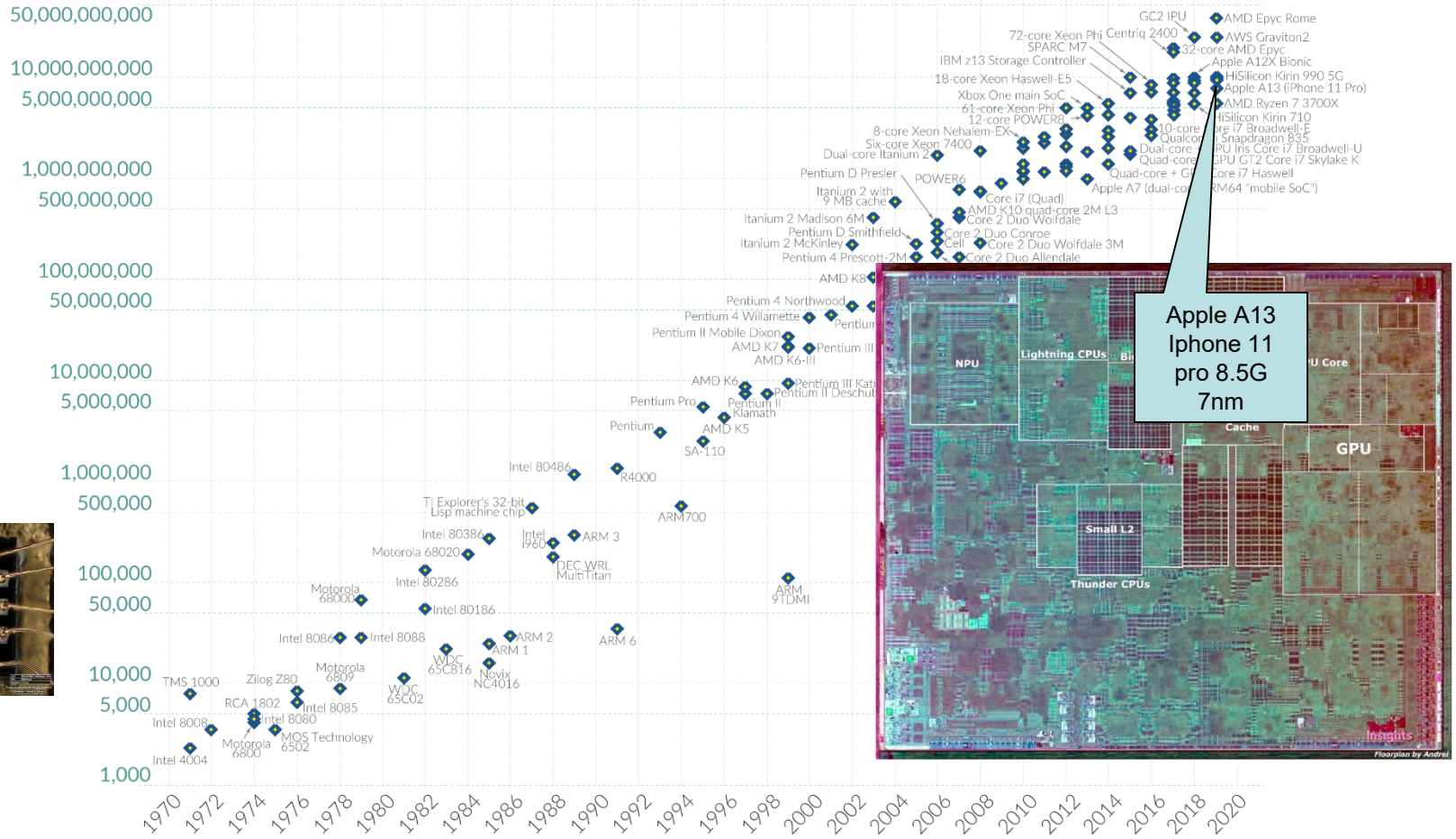

Gate
Isolator
Bulk
Source
Drain
P-Si


VDD = 1.2
GND = 0

Moore's Law: The number of transistors on microchips doubles every two years

Our World in Data

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years.
This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.



source: Wikipedia (wikipedia.org/wiki/Transistor_count)
OurWorldInData.org – Research and data to make progress against the world's largest problems

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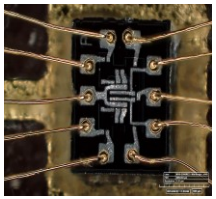
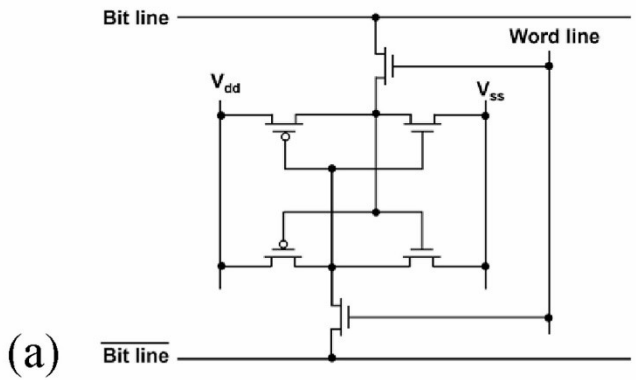
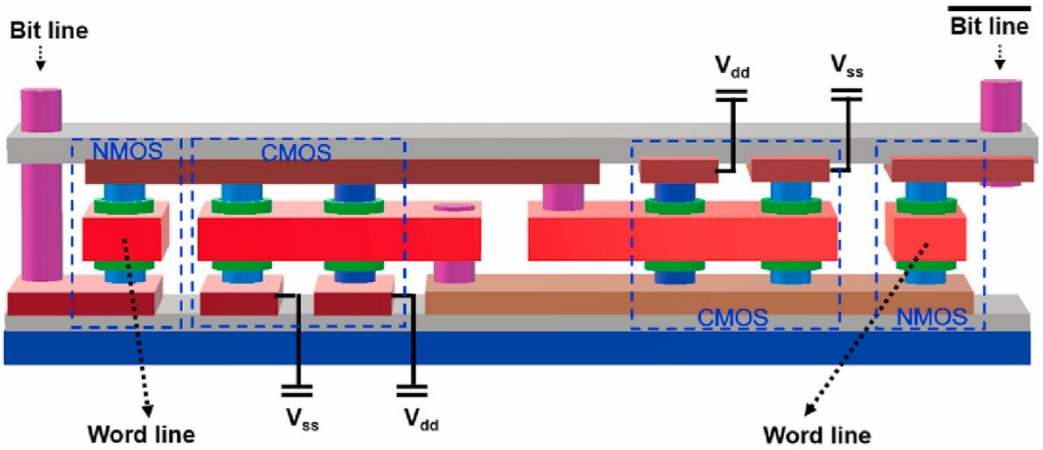


One of first CMOS ICs

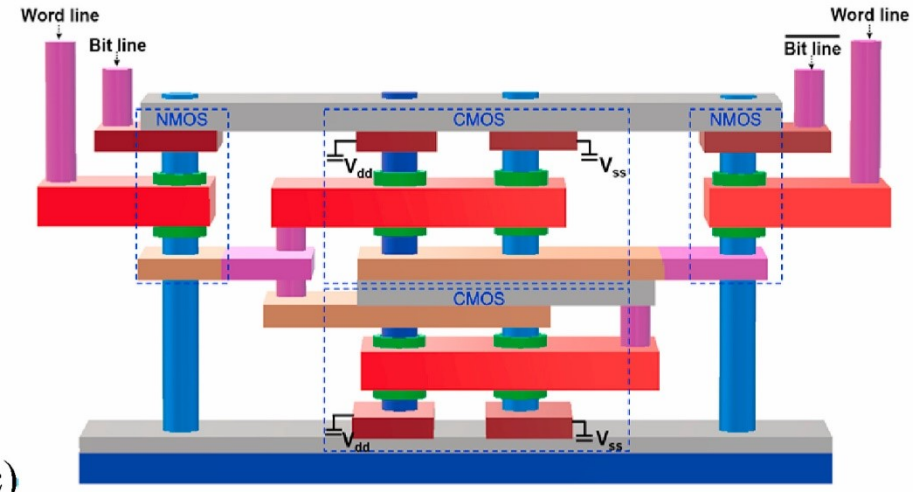
Moore: Since 1970, the number of transistors on a chip has doubled every 18 months


Bit line
Word line
V_{dd}
V_{ss}
Bit line

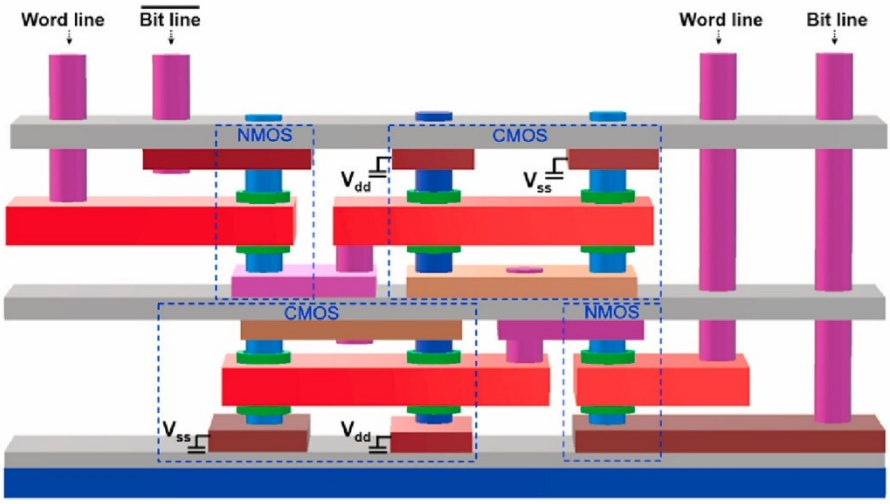
(a)


Bit line
Bit line
V_{dd}
V_{ss}
NMOS
CMOS
CMOS
NMOS
Word line
V_{ss}
V_{dd}
Word line

(b)


Word line
Bit line
Word line
Bit line
NMOS
CMOS
NMOS
V_{dd}
V_{ss}
CMOS
V_{dd}
V_{ss}

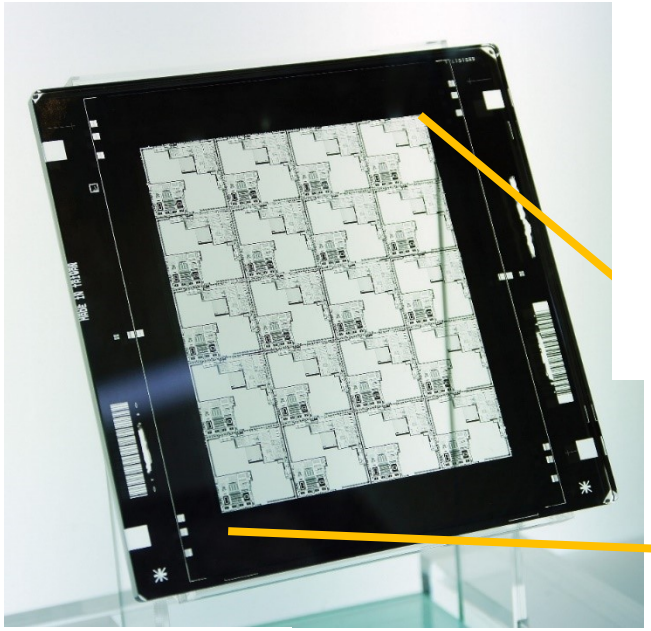
(c)


Word line
Bit line
Word line
Bit line
NMOS
CMOS
V_{dd}
V_{ss}
CMOS
NMOS
V_{ss}
V_{dd}

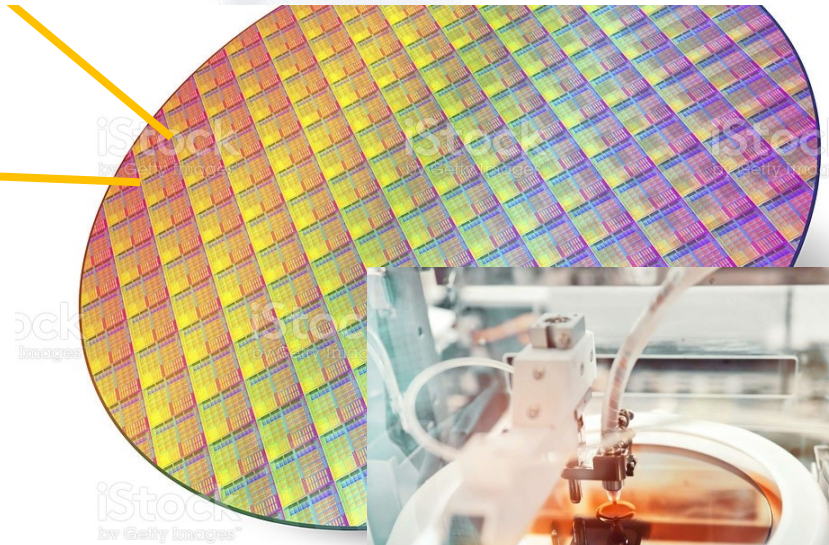
(d)

Technology

Projektor (stepper)

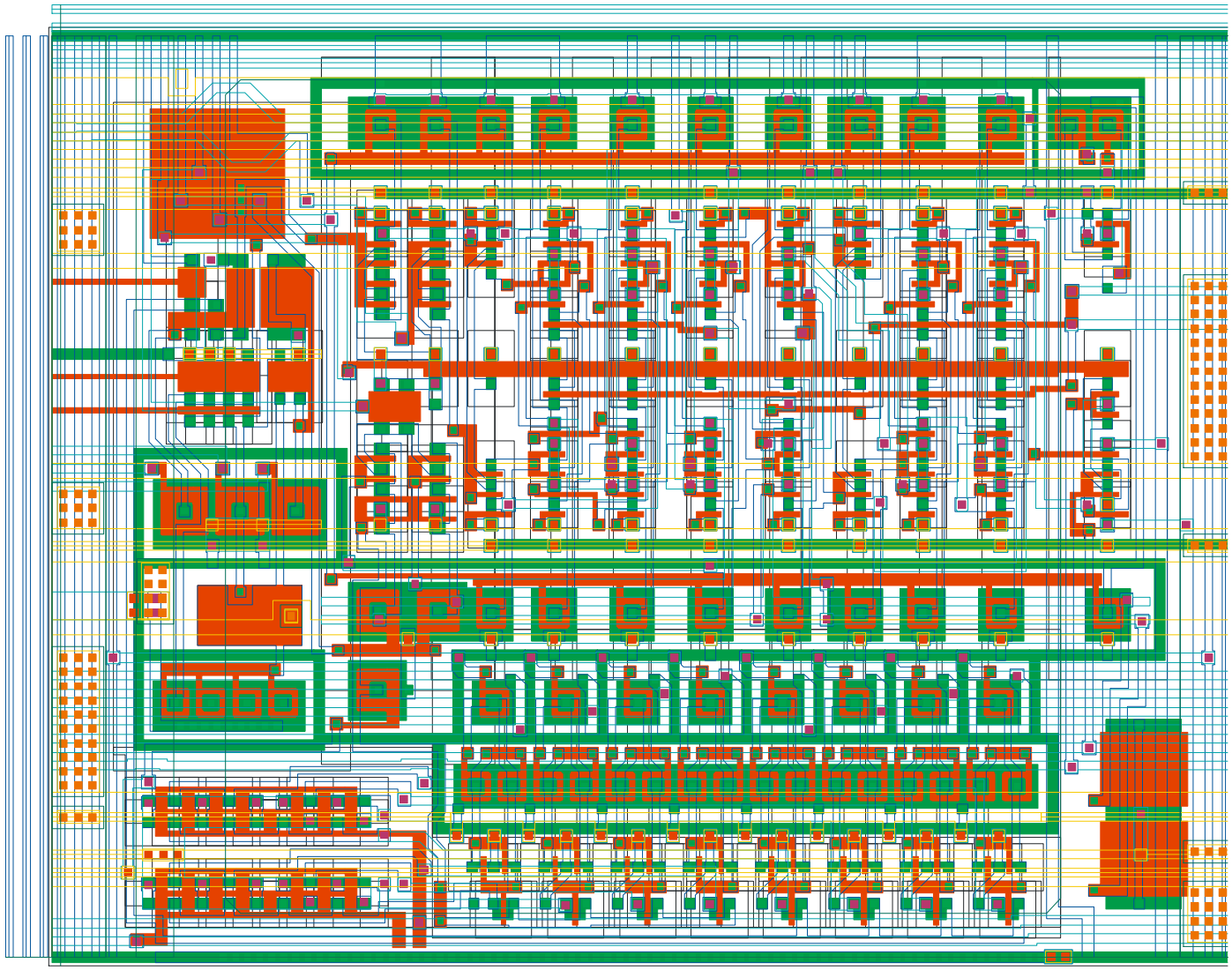


Fotomaske



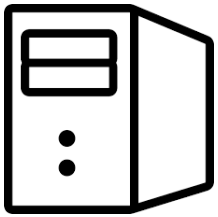
Wafer

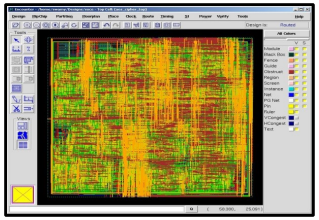
Layout

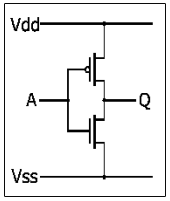


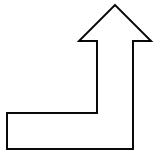
Digital and analog design flows

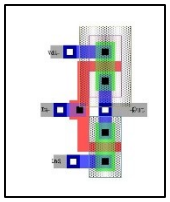
Digital design flow



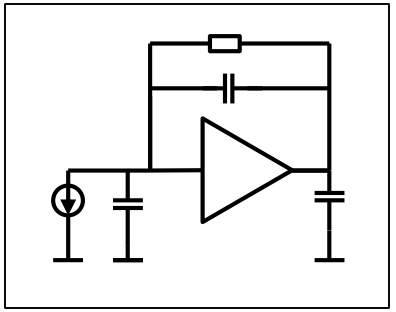


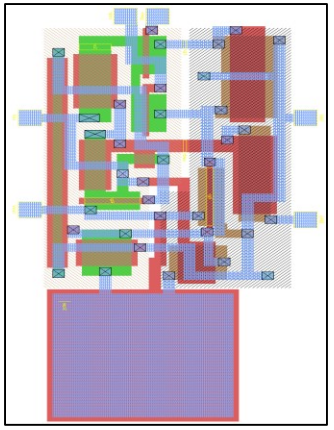




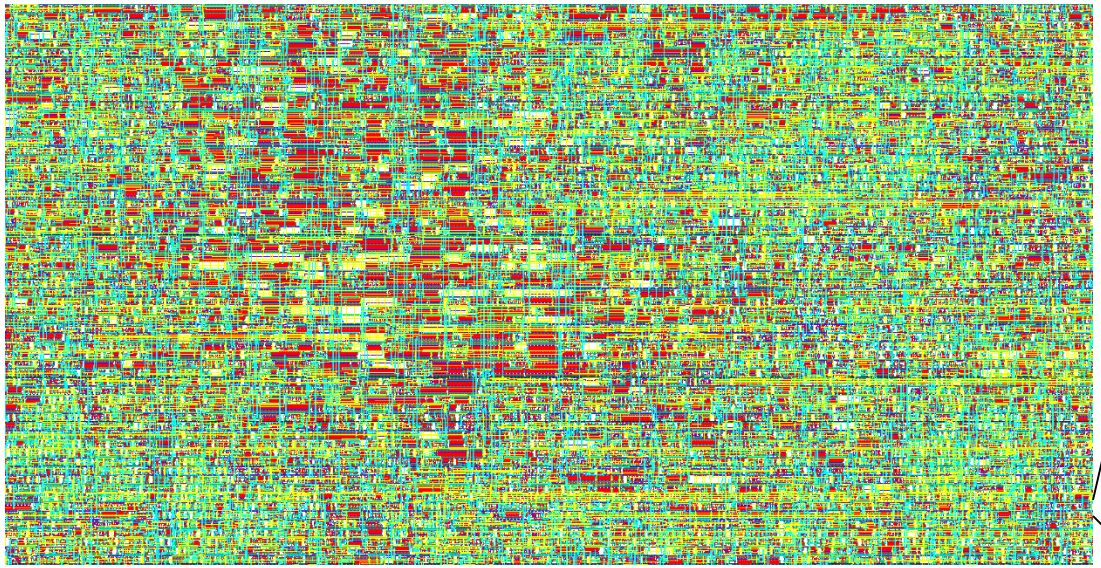


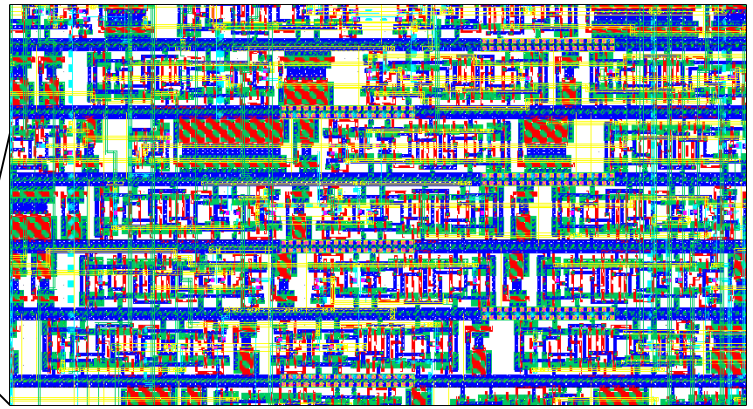
Analog design fow

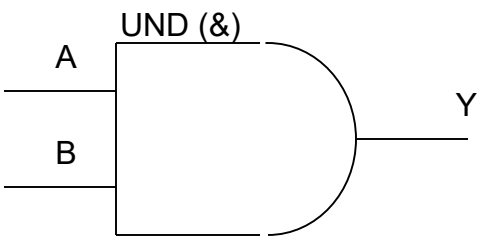


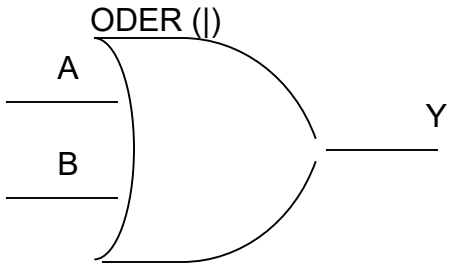


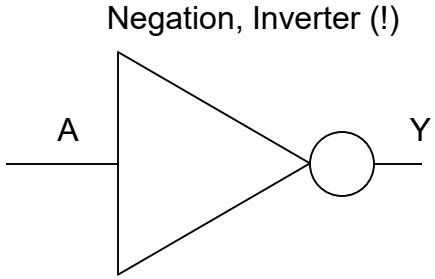
Digital design flow



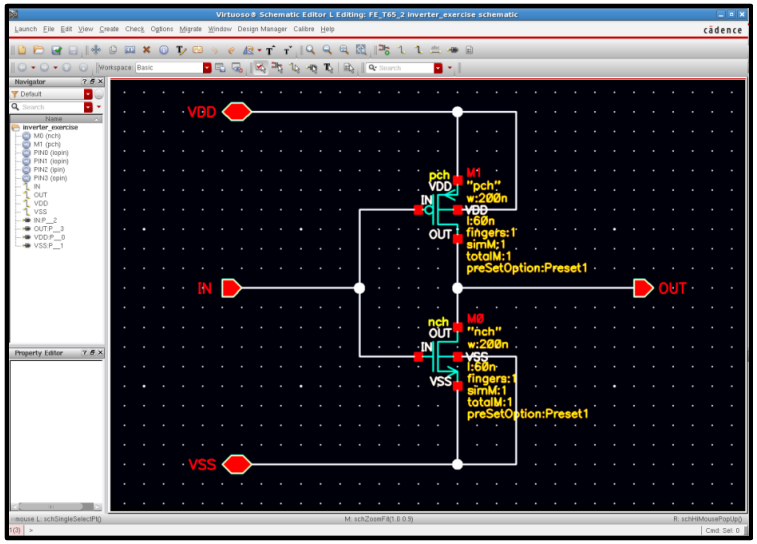



UND (&)
A
B
Y

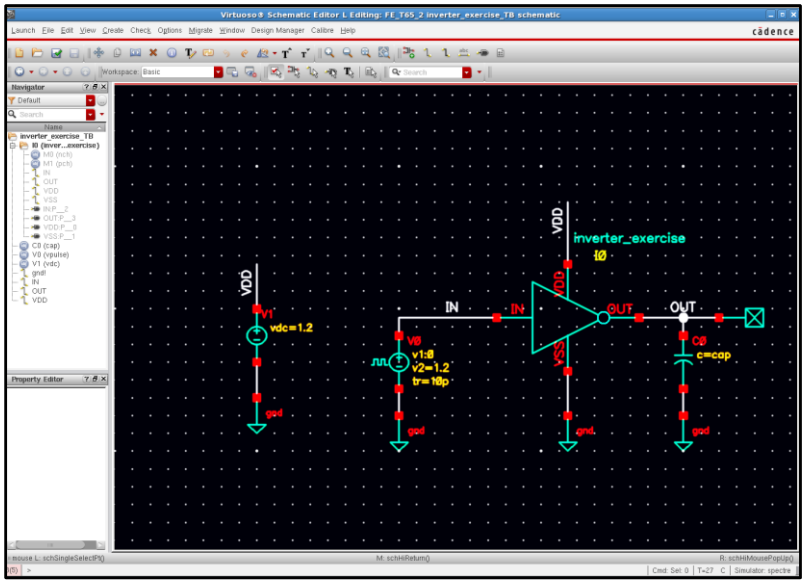

ODER (|)
A
B
Y

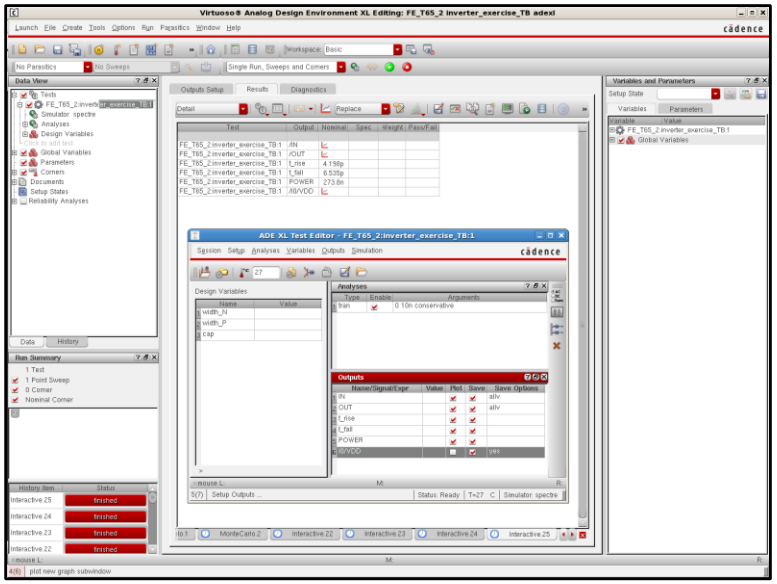

Negation, Inverter (!)
A
Y

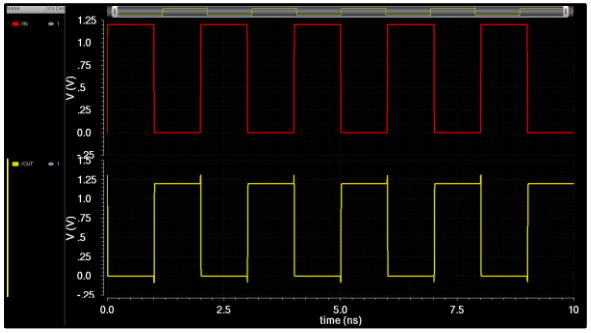
Schematic


VDD
pch
VDD
IN
OUT
M1
"pch"
w:200n
l:60n
fingers:1
simM:1
totalM:1
preSetOption:Preset1
IN
OUT
nch
OUT
IN
VSS
M0
"nch"
w:200n
l:60n
fingers:1
simM:1
totalM:1
preSetOption:Preset1
VSS

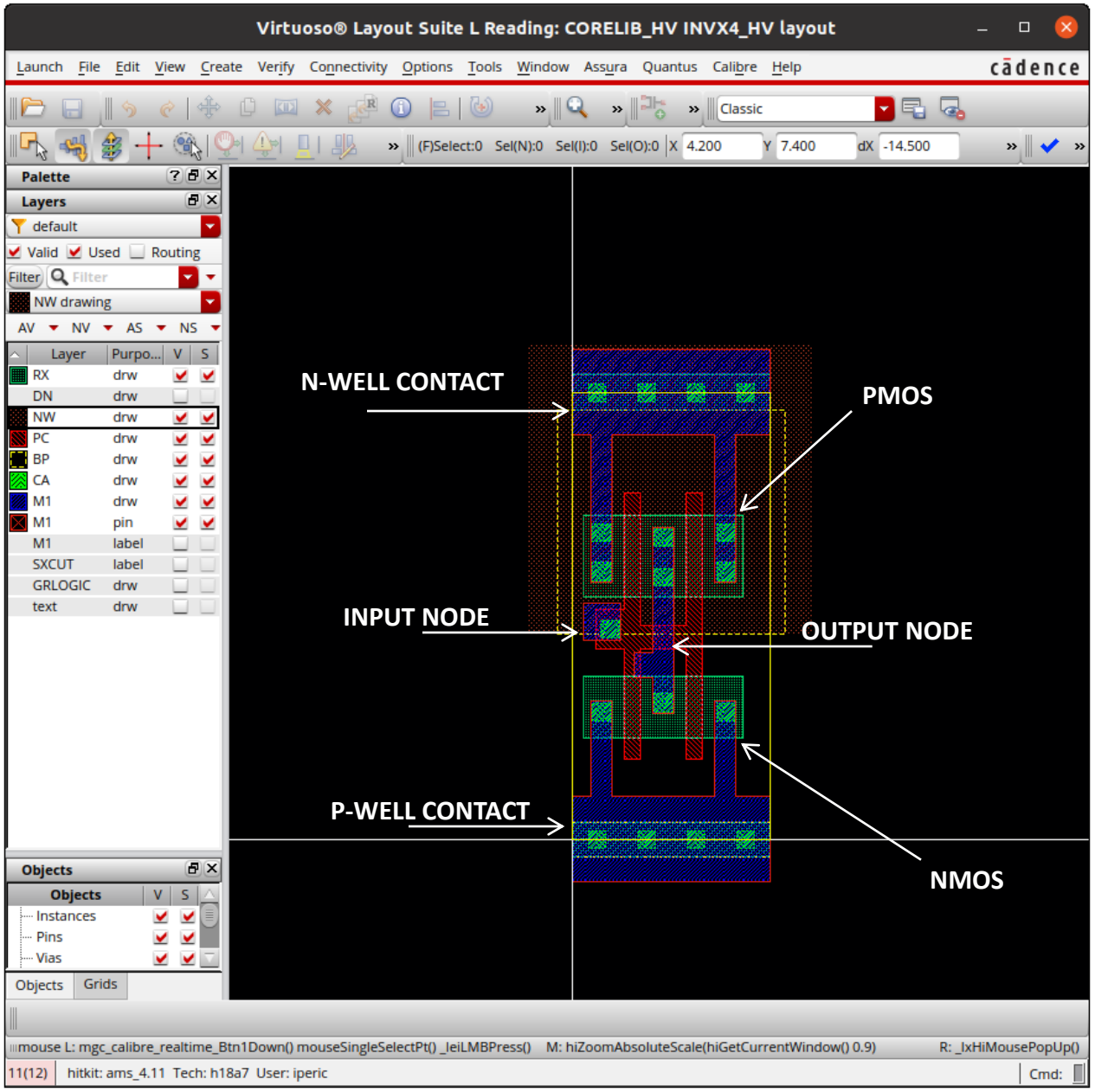
Simulation


Virtuoso® Schematic Editor L Editing: FE_T65_2 inverter_exercise_TB schematic
inverter_exercise
VDD
IN
OUT
vdc=1.2
v1=0
v2=1.2
tr=10p
c=cap
gnd


Virtuoso® Analog Design Environment XL Editing: FE_T65_2 inverter_exercise_TB adexl
ADE XL Test Editor - FE_T65_2:inverter_exercise_TB:1


V (V)
time (ns)
0.0
2.5
5.0
7.5
10

Layout


Virtuoso® Layout Suite L Reading: CORELIB_HV INVX4_HV layout
N-WELL CONTACT
PMOS
INPUT NODE
OUTPUT NODE
P-WELL CONTACT
NMOS

Code

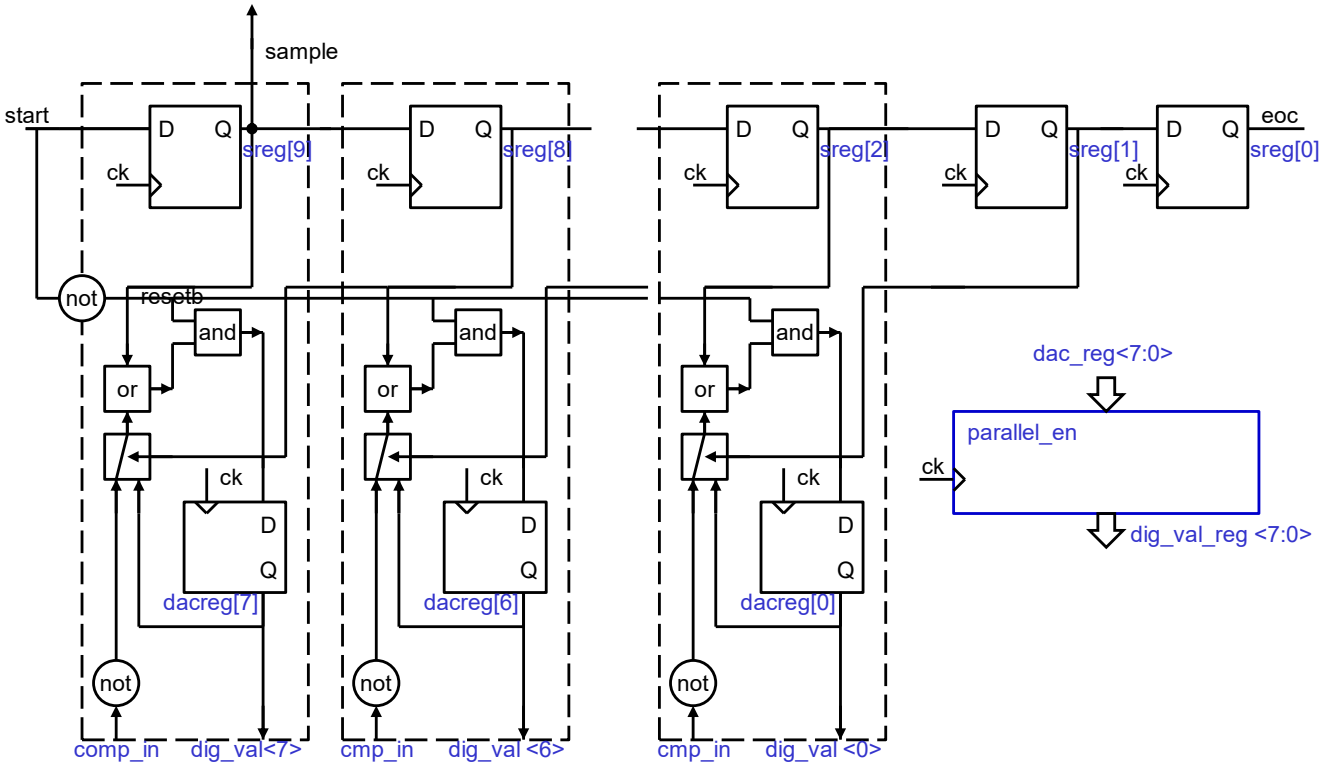
```
module ADC_digital_v (

input comp_in,
input start,clk,rst_n,
output [7:0] dig_val,
output sample,
output sampleb,
output eoc,
output reg [7:0] dig_val_reg
);


reg [9:0] sreg;
reg [7:0] dacreg;
assign sample = sreg[9];
assign sampleb = ~sreg[9];
assign eoc = sreg[0];
assign dig_val = dacreg;
wire reset;
assign reset = start;


always @(posedge clk or negedge rst_n) begin
if (~rst_n) begin
                sreg <= 10'd0;
                dacreg <= 8'd0;
end
else begin
                sreg[9:0] <= {start,sreg[9:1]};
                if(eoc) dig_val_reg <= dacreg;
                if(reset == 1) dacreg[7:0] <= 0;
                else dacreg[7:0] <= sreg[9:2] | ( (sreg[8:1] &  {8{~comp_in}} ) | (~sreg[8:1] & dacreg[7:0]) );
end//no reset
end//alw

endmodule
```

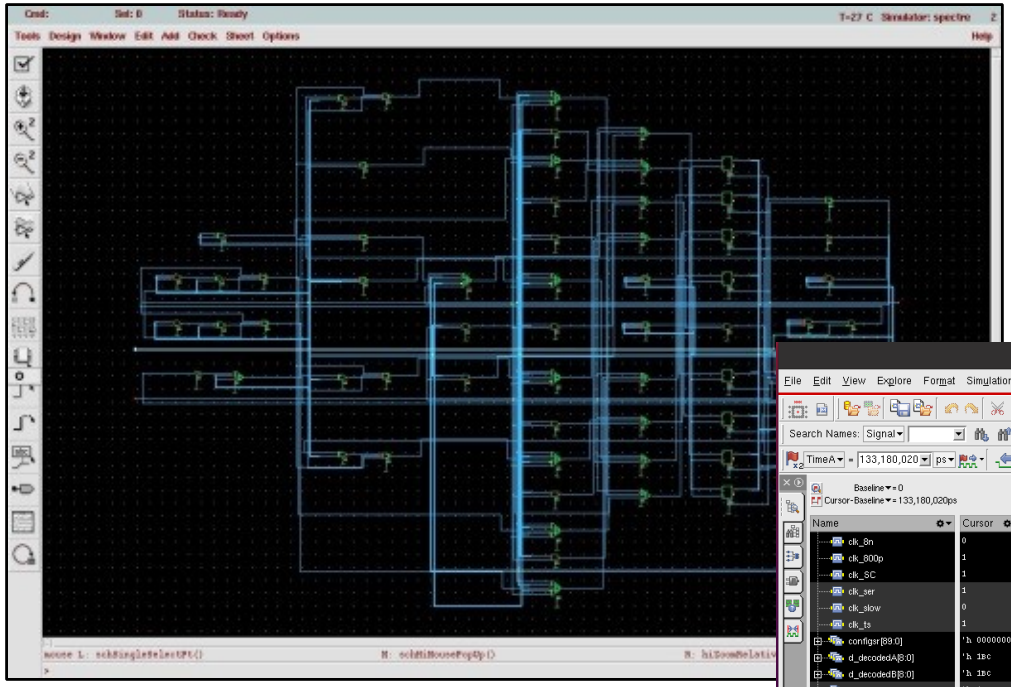


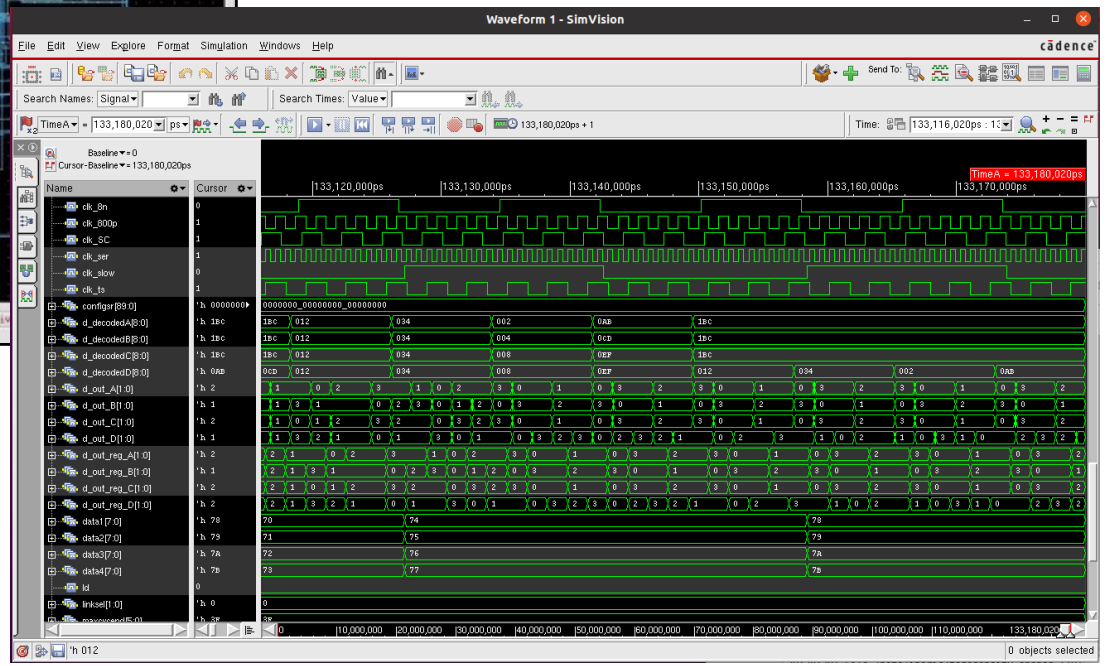
code that describes shift register

output register

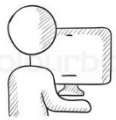
Not very readable line with bitwise operations that describes the combinatorial connections between sreg and dacreg

Netlist



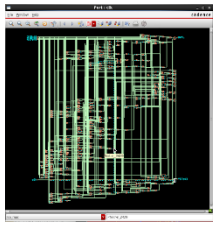

Waveform 1 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Search Names: Signal
Search Times: Value
Name
Cursor
clk_8n
clk_800p
clk_SC
clk_ser
clk_slow
clk_ts
configsr[89:0]
d_decodedA[8:0]
d_decodedB[8:0]
d_decodedC[8:0]
d_decodedD[8:0]
d_out_A[1:0]
d_out_B[1:0]
d_out_C[1:0]
d_out_D[1:0]
d_out_reg_A[1:0]
d_out_reg_B[1:0]
d_out_reg_C[1:0]
d_out_reg_D[1:0]
data1[7:0]
data2[7:0]
data3[7:0]
data4[7:0]
ld
linkset[1:0]
133,120,000ps
133,130,000ps
133,140,000ps
133,150,000ps
133,160,000ps
133,170,000ps
TimeA = 133,180,020ps
0 objects selected

Synthesis

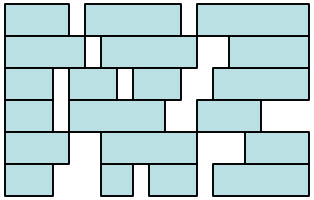


Code

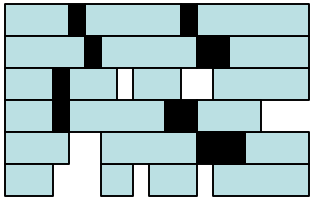
Netlist



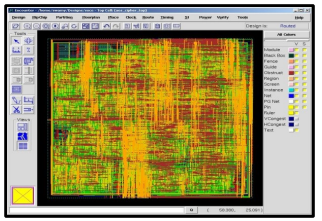
Placing

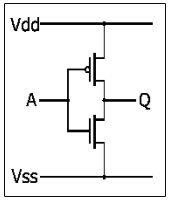


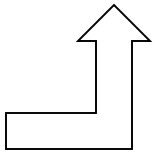
Clock tree

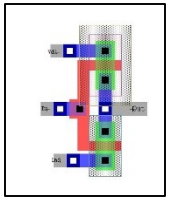


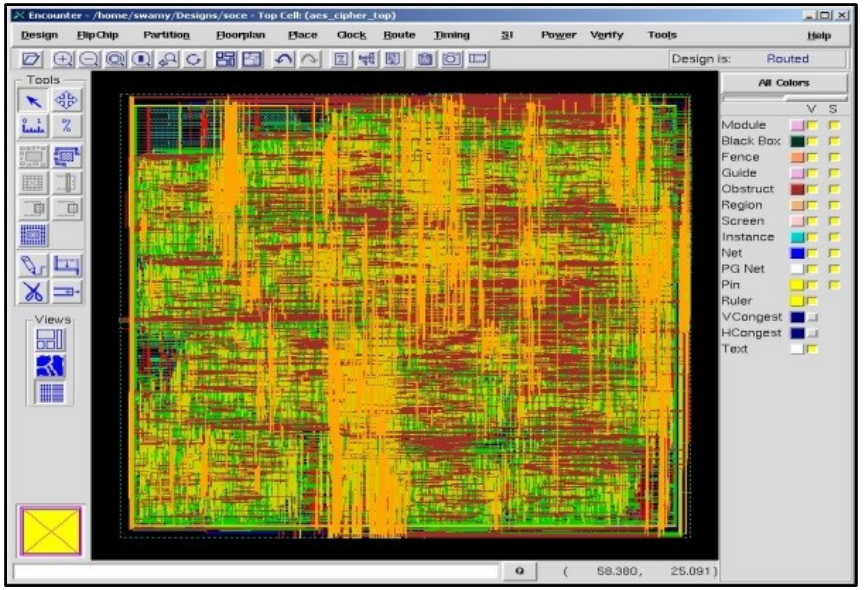
Routing





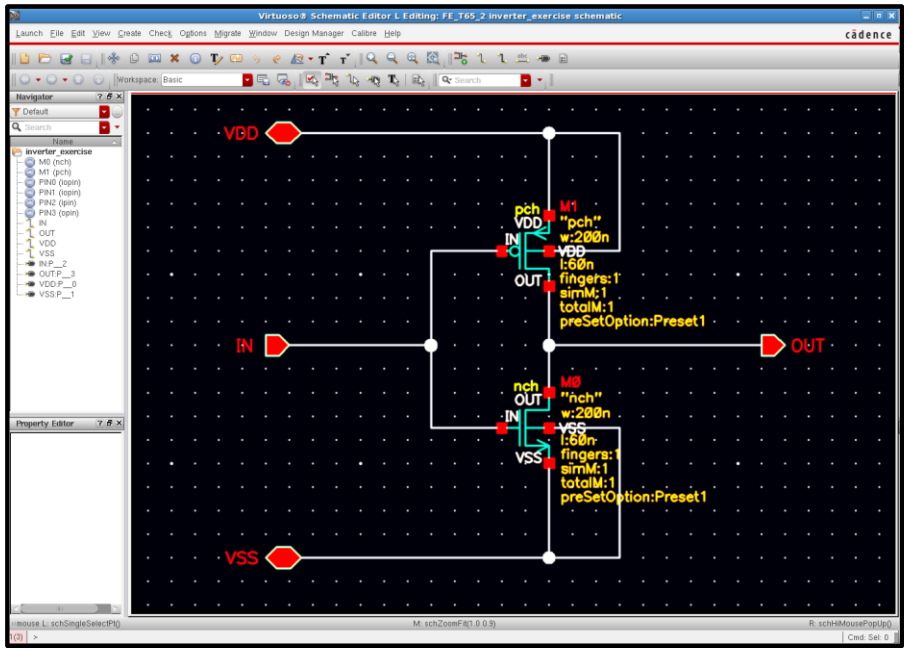


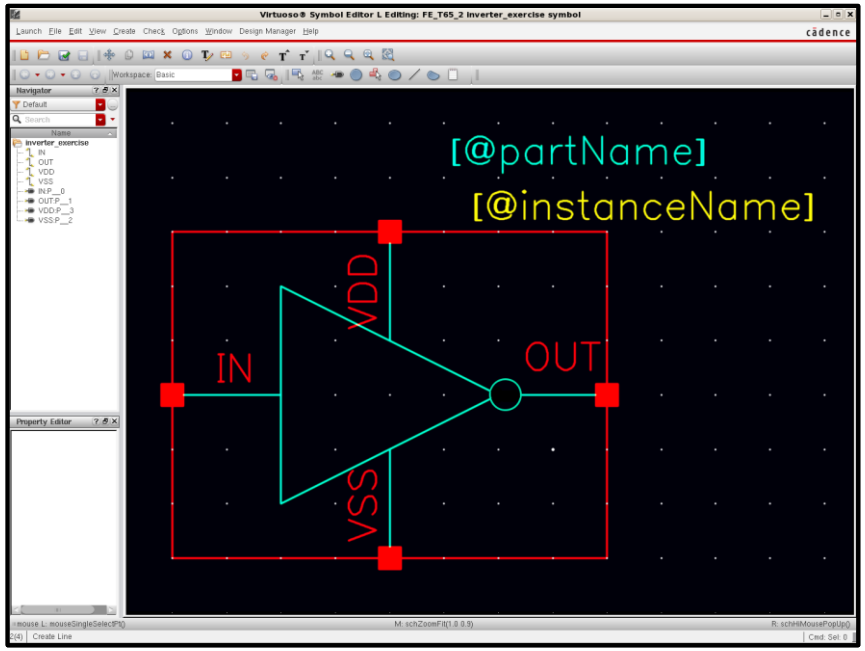




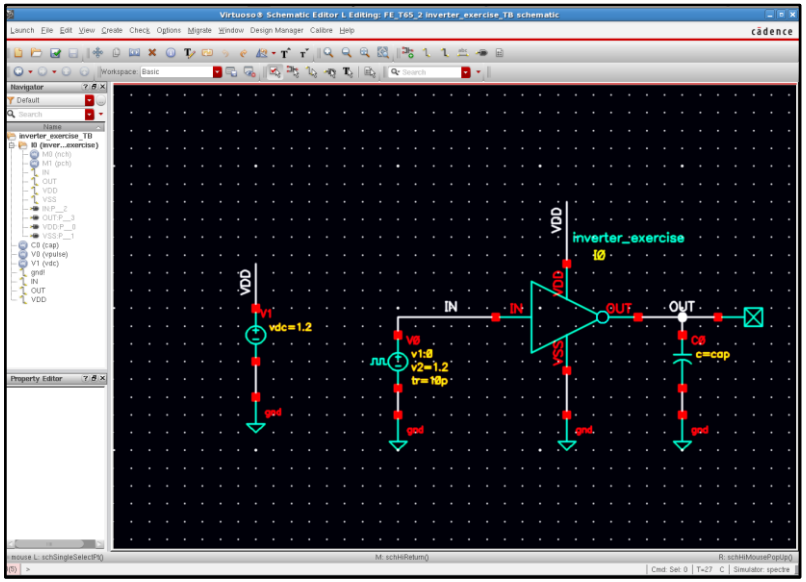
Analog design flow

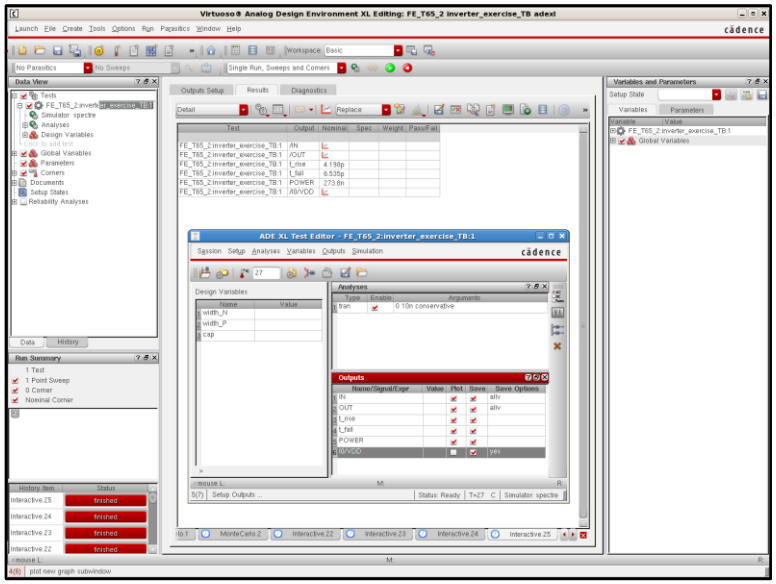
Analog Design Flow - Schematic

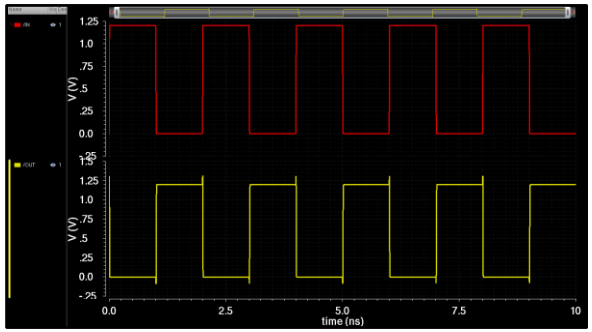


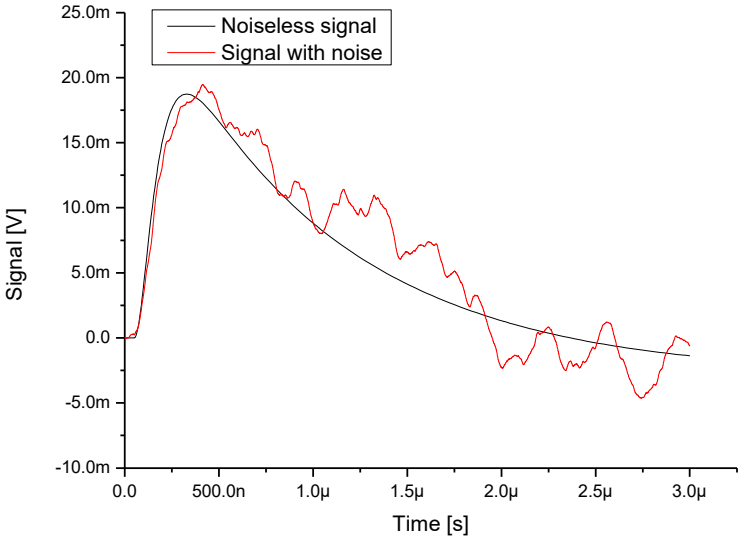


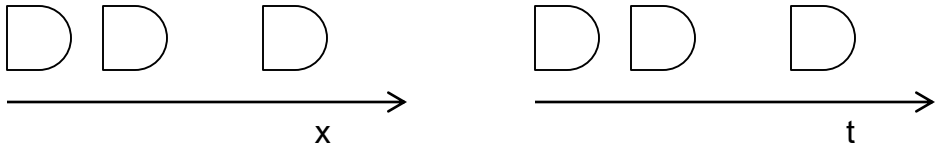
Analog Design Flow - Simulation

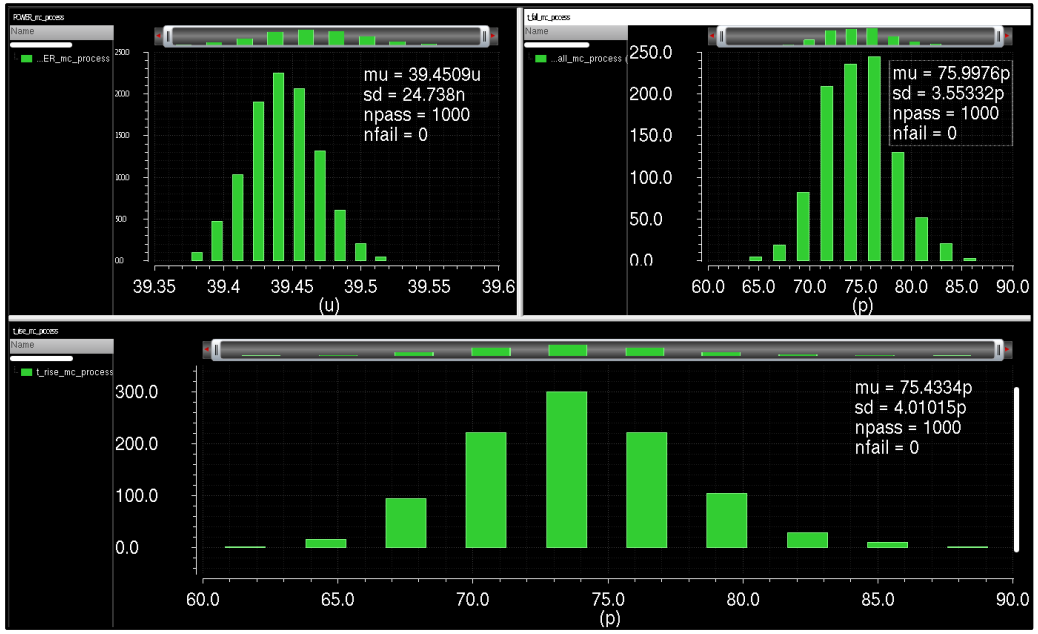




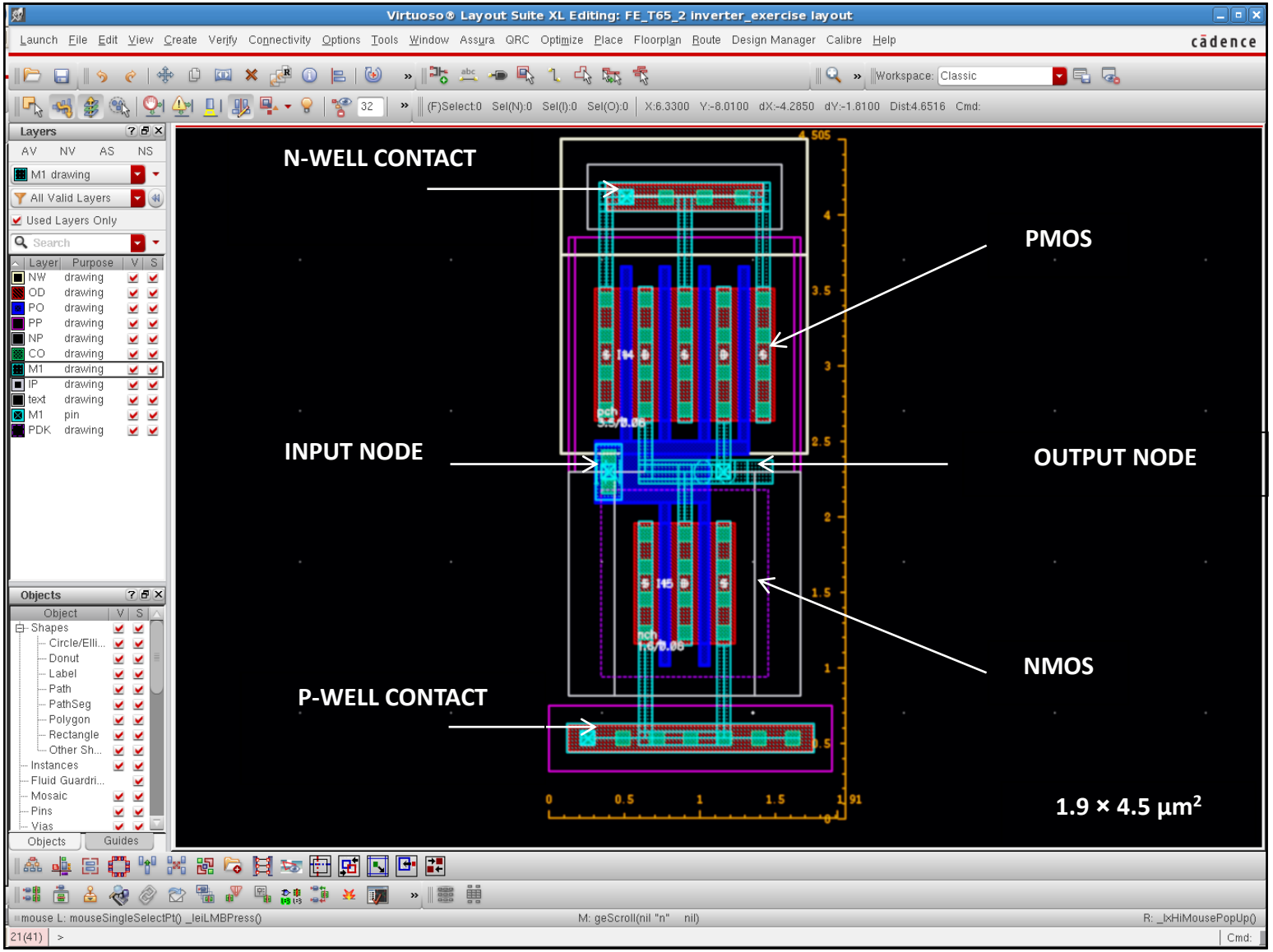



Noiseless signal
Signal with noise
Signal [V]
Time [s]
25.0m
20.0m
15.0m
10.0m
5.0m
0.0
-5.0m
-10.0m
0.0
500.0n
1.0µ
1.5µ
2.0µ
2.5µ
3.0µ


x
t

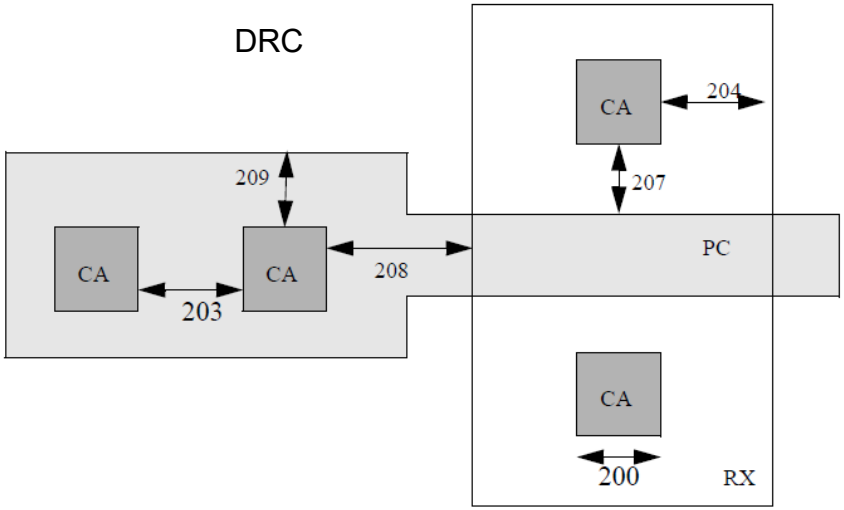

mu = 39.4509u
sd = 24.738n
npass = 1000
nfail = 0
39.35
39.4
39.45
39.5
39.55
39.6
(u)
mu = 75.9976p
sd = 3.55332p
npass = 1000
nfail = 0
60.0
65.0
70.0
75.0
80.0
85.0
90.0
(p)
mu = 75.4334p
sd = 4.01015p
npass = 1000
nfail = 0
300.0
200.0
100.0
0.0
(p)

Analog Design Flow - Layout

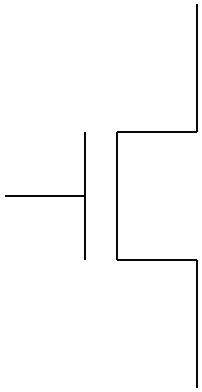


Analog Design Flow - Layout

- Layout rules (part of PDK)
- DRC review of layout rules
- Avalanche Layout Schematic Comparison
- Layout -> Netlist <-> Netlist <- Schematic
- Extraction of capacities from layout
- Post-Layout Simulation
- Adaptation of the circuit diagram necessary

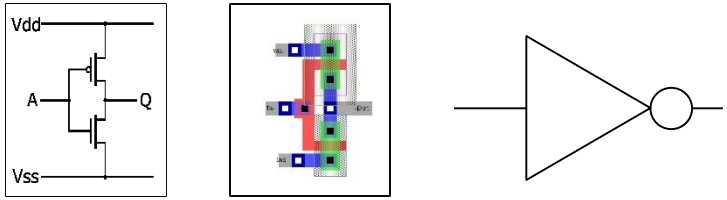


LVS



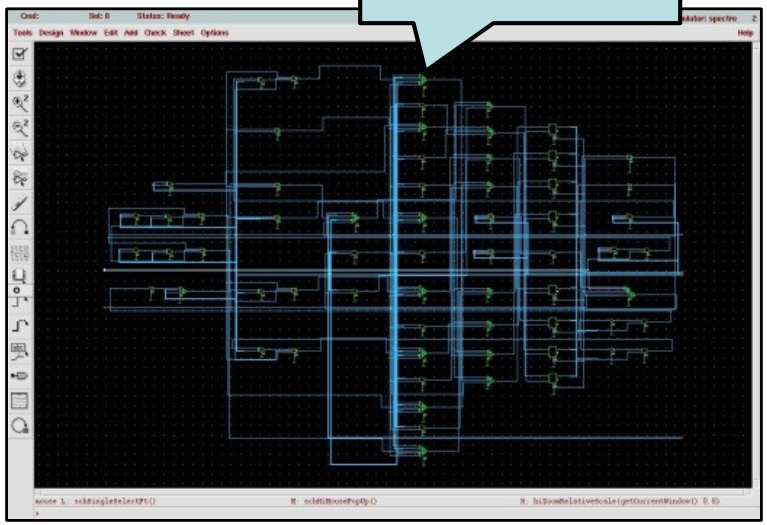
Cells and views

A basic cell: inverter

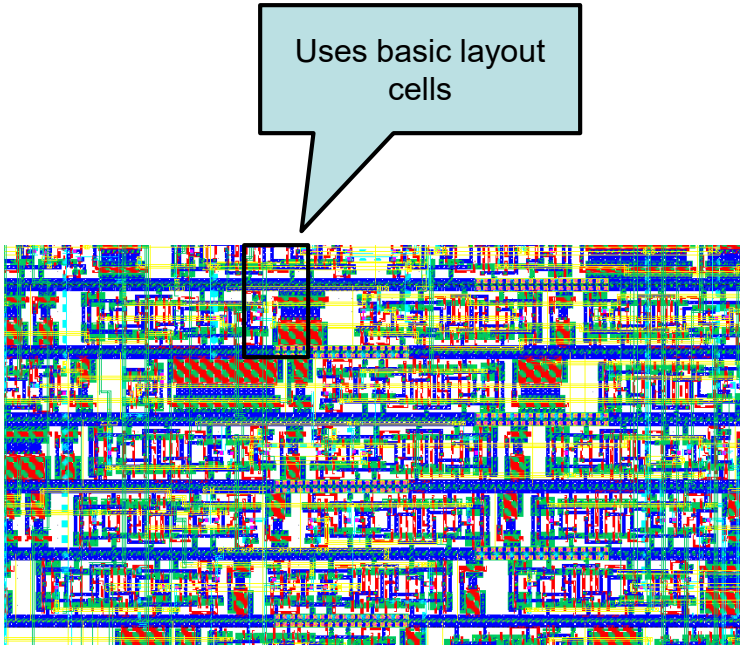


Views of a cell: Inverter.schematic Inverter.layout Inverter.symbol

Complex cell Controller



Controller.schematic



Controller.layout

Cells and views

- In the case of analog circuits, the lowest level in the hierarchy contains the components: NMOS, PMOS transistor, capacitor, and resistor. These basic components are the instances (copies) of corresponding cells.
- In the case of digital circuits, the basic components are the instances of logical gates and the memory components (AND, OR, inverter, flip-flop).
- Although a chip has billions of transistors (billions of instances, copies), the number of cells is not large.

Foundries

- Foundries and processes

UMC

TSMC

TSI semiconductors

Globalfoundries

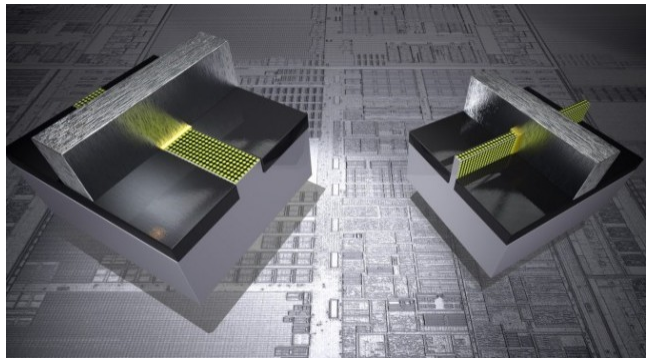
Lfoundry

AMS

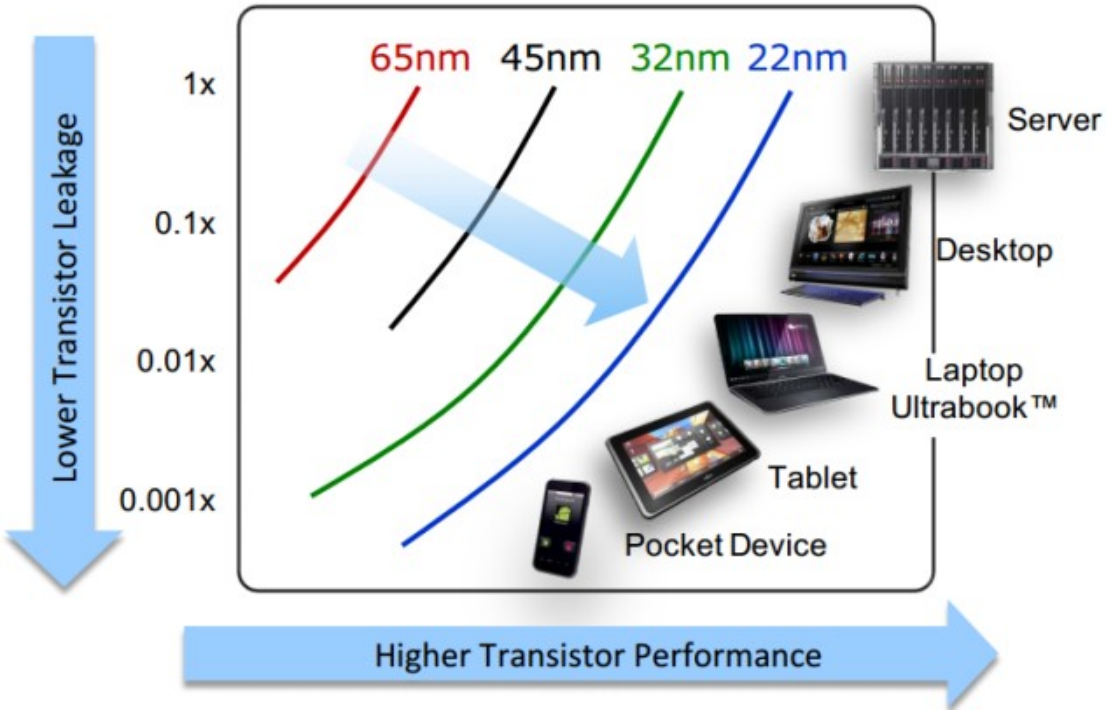
IHP

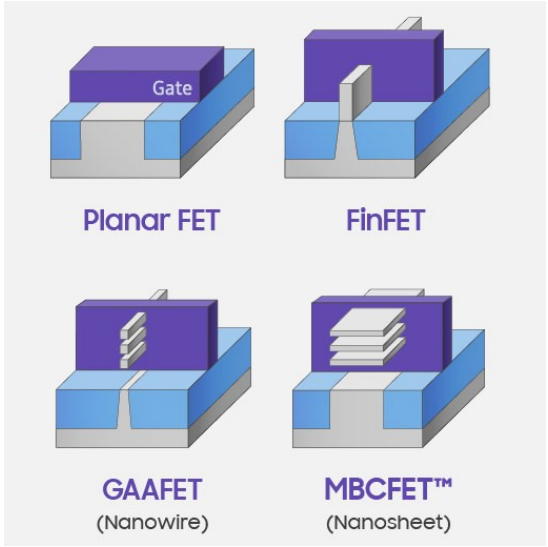
Processes

- Opto CMOS, HVCMOS, SOI, BiCMOS
- FinFET, Fully Depleted SOI, nanowire Gate all around
- Process nodes:
- 0.35µm, 0.18µm, 0.13µm, 0.11µm, 90, 65, 55, 40, 28, 22, 16, 12, 7, 6, 5nm



http://www.extremetech.com/





https://www.cnx-software.com/2019/05/17/mbcfet-process-technology-3nm-processors/

- Europractice: Multi Project Runs und Design Support
- http://europractice-ic.com/
- Offers:
- Foundry access
- Software download
- Software Licenses
- Engineering runs
- MPW runs
- https://europractice-ic.com/mpw-prototyping/general/mpw-minisic/
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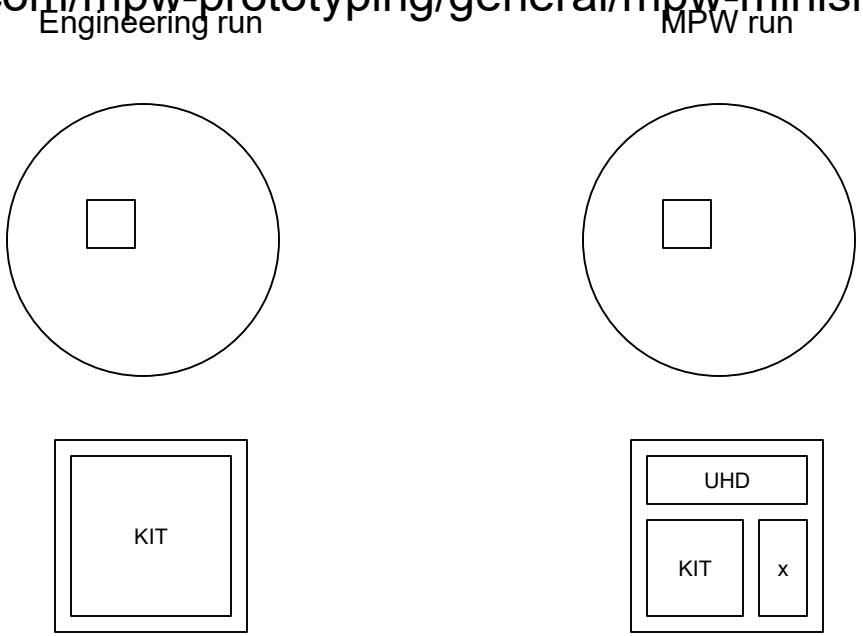
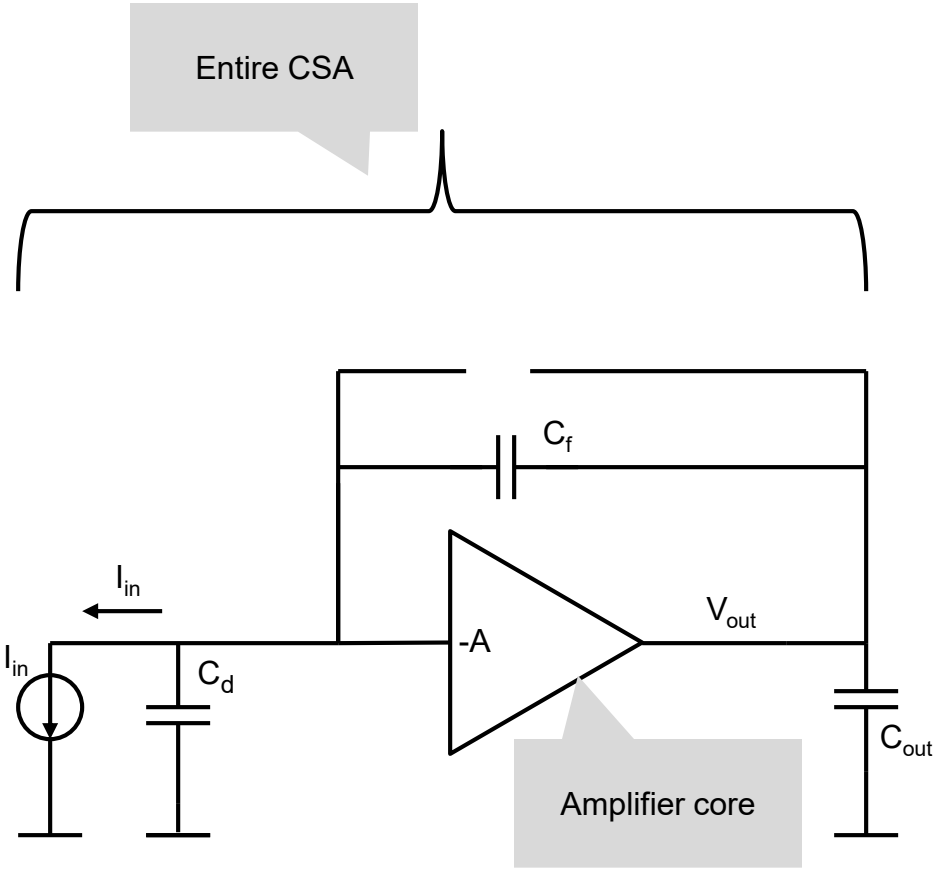


Charge sensitive amplifier

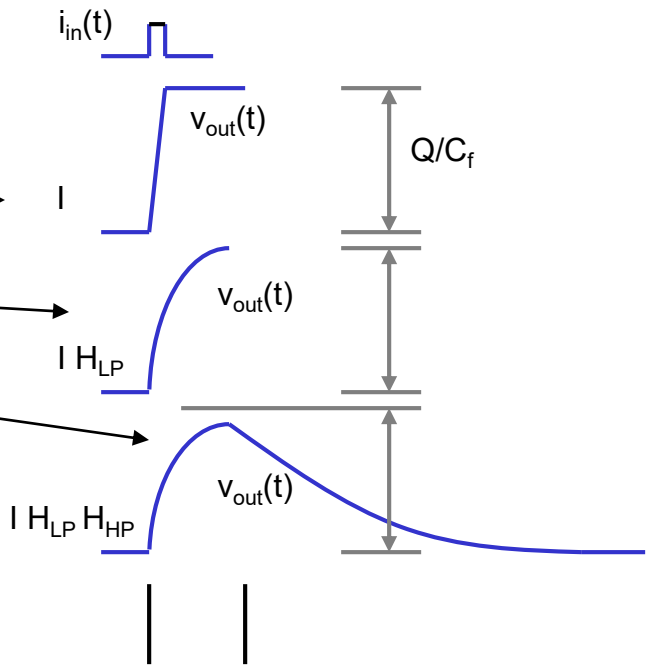
Charge sensitive amplifier - theory

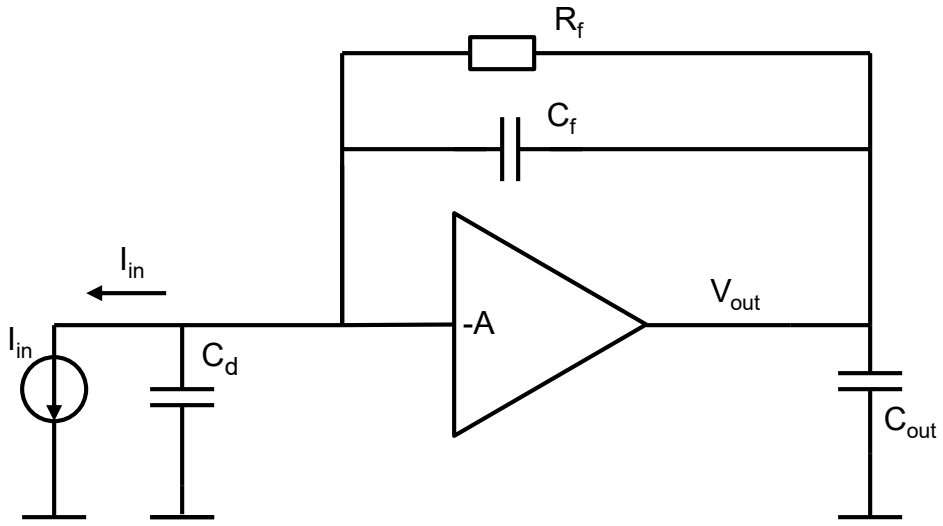
- Charge sensitive amplifier (CSA) consists of a voltage amplifier (“amplifier-core”) with negative voltage amplification -A and feedback circuit (capacitance C_f)
- Ideal CSA works as an integrator, the output voltage is integral of the input current multiplied by $1/C_f$
- Therefore, the ideal CSA has the charge amplification
- $A_Q = \frac{V_{out,max}}{Q_{in}} = \frac{1}{C_f}$
- V_{out} is the amplitude of the output signal



Charge sensitive amplifier - theory

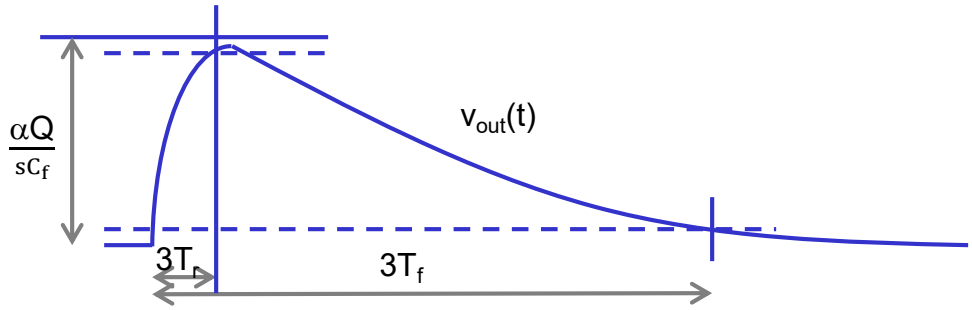
- Realistic CSA with R_f and C_f in feedback has the following transfer function (s is complex frequency):
- $\frac{V_{out}(s)}{I_{in}(s)} = \frac{\alpha}{sC_f}\frac{1}{(sT_r+1)}\frac{sT_f}{(sT_f+1)} \equiv \frac{\alpha}{sC_f} H(s)_{LP} H(s)_{HP}$ (1)
- Transfer function part $\frac{\alpha}{sC_f}$ describes the integrator
- $\frac{1}{(sT_r+1)} \equiv H_{LP}(s)$ is the function of a low pass filter
- $\frac{sT_f}{(sT_f+1)} \equiv H_{HP}(s)$ describes a high pass filter
- Therefore realistic CSA is a combination of an integrator with gain α/C_f, low pass- and high pass filter
- Such a CSA is an integrator and a filter in one component
- Factor α is equal to
- $\alpha = \frac{\beta A}{1+\beta A}$, with $\beta = \frac{C_f}{C_f+C_d}$ and A voltage amplification (2)



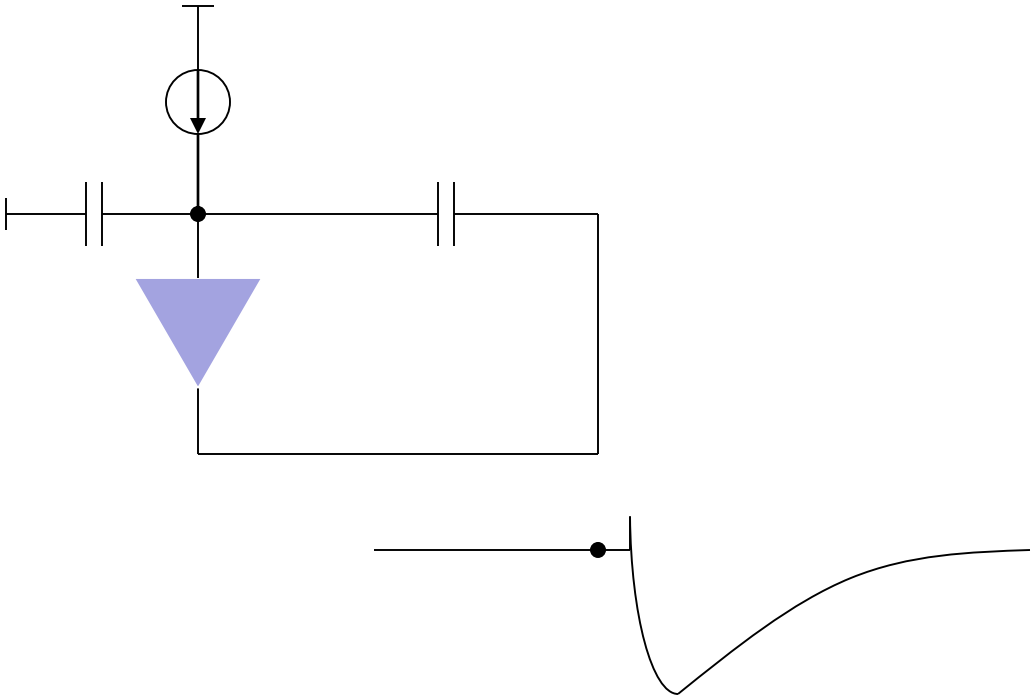


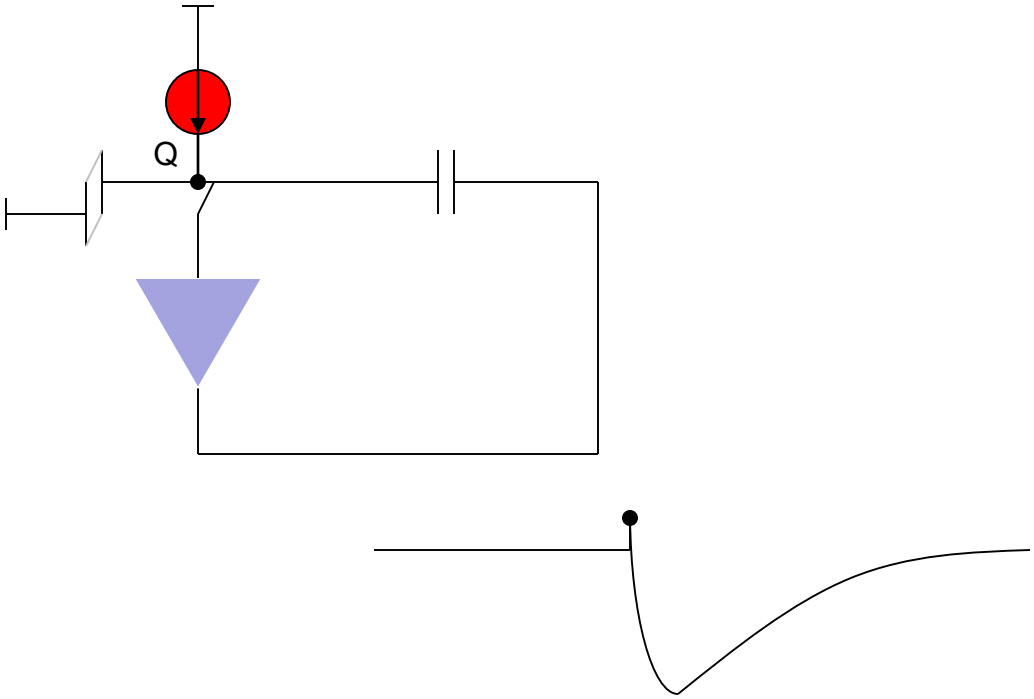
Time constants

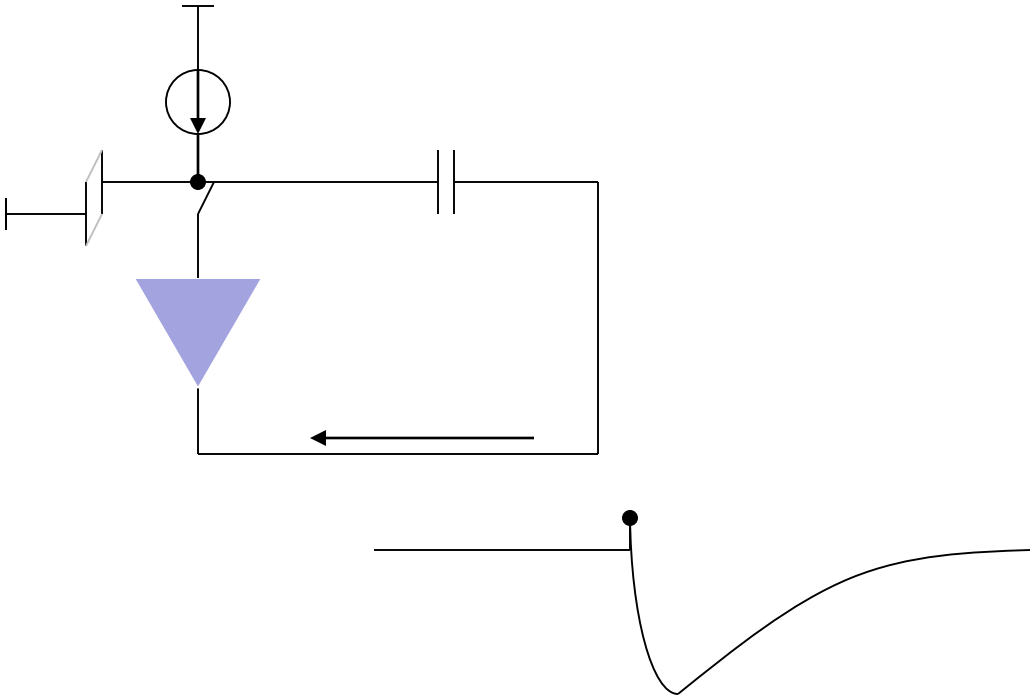
- The response to charge pulse has two time constants, T_r and T_f
- T_r is the rise time constant and T_f is the fall time constant
- In a system with one time constant, the rise time from 0 to 95% of the maximum amplitude takes three time constants
- If $T_f >> T_r$, the pulse has the asymmetric shape and $V_{max} \sim \frac{\alpha Q}{sC_f}$

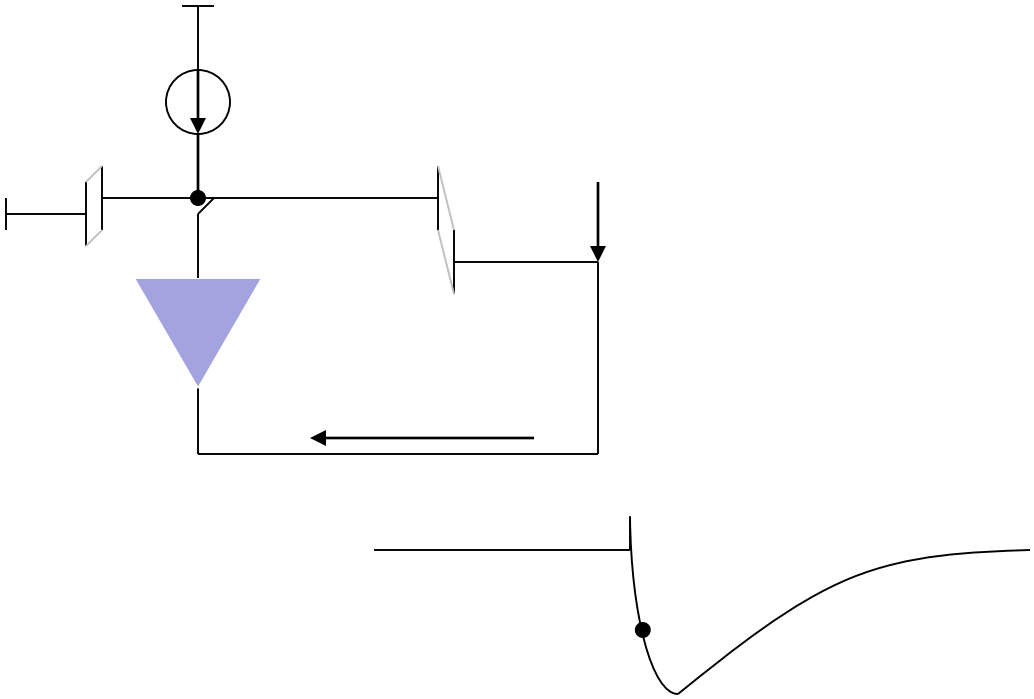


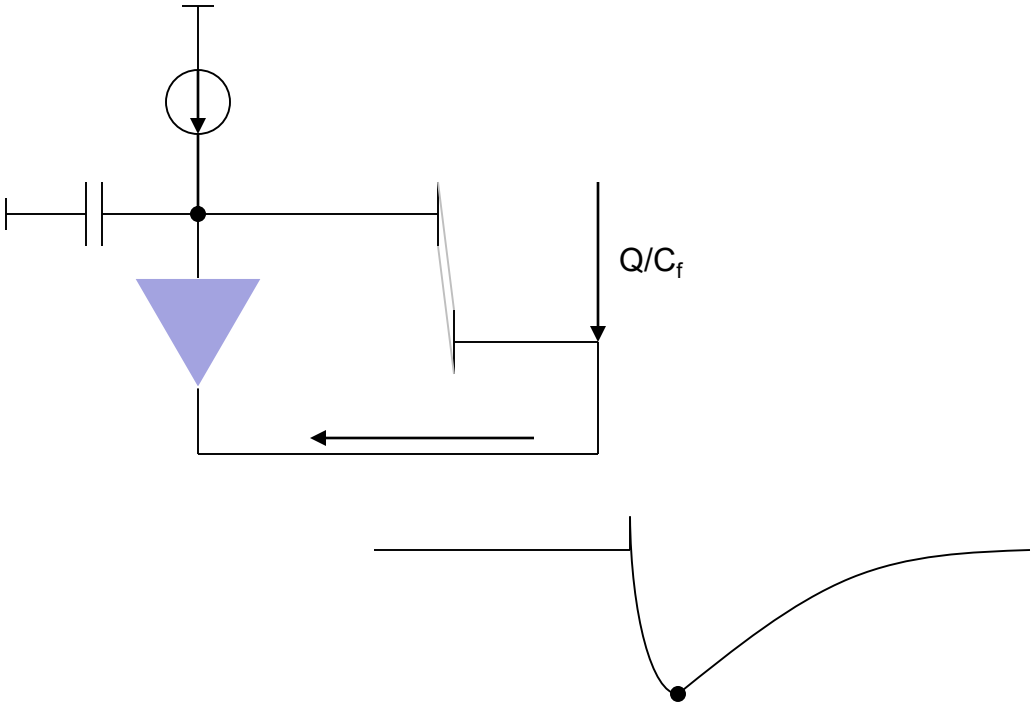
- Animation

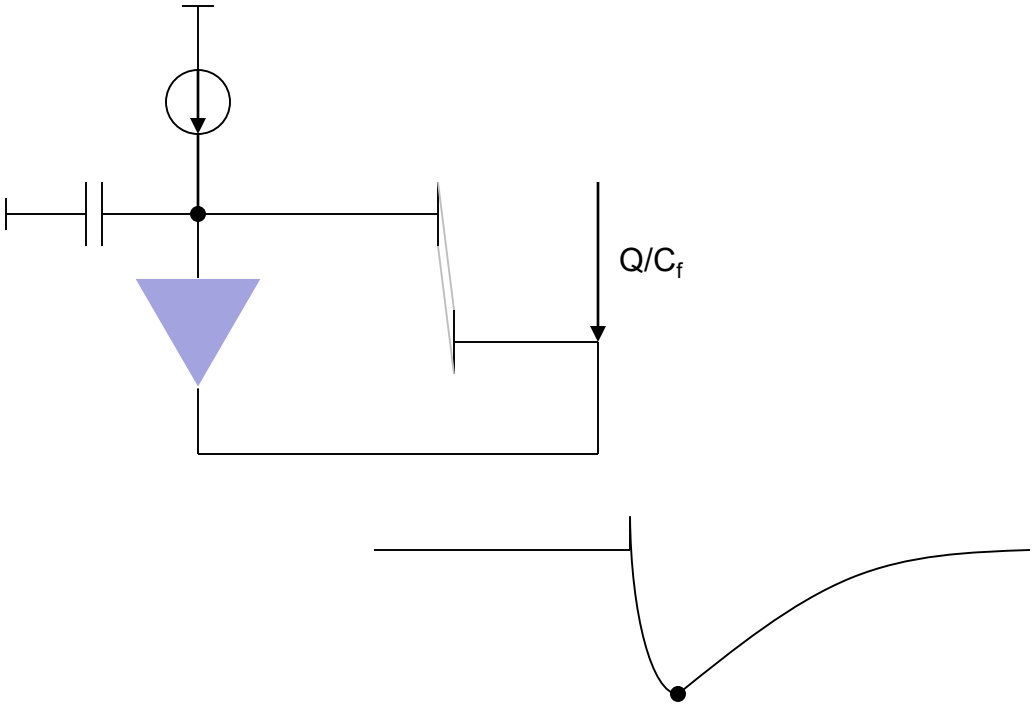


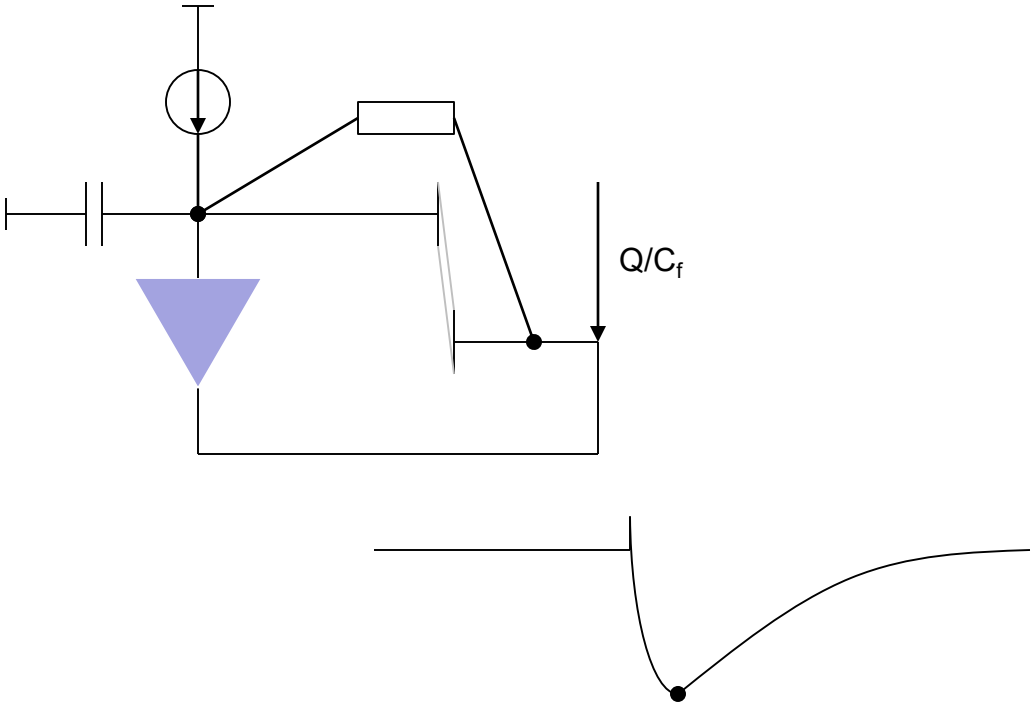

Q

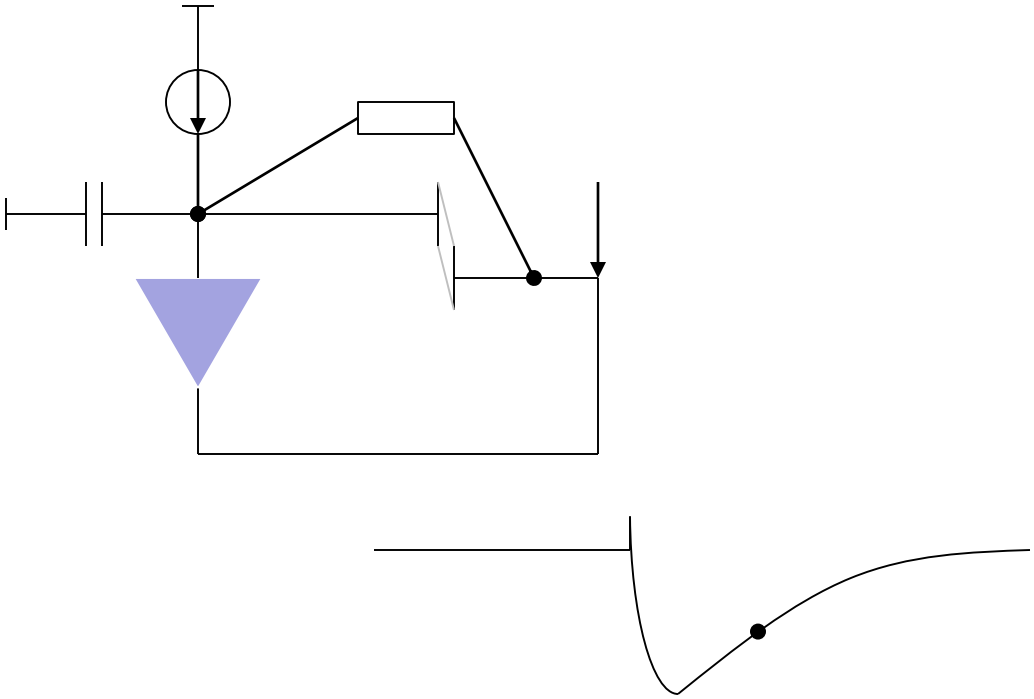


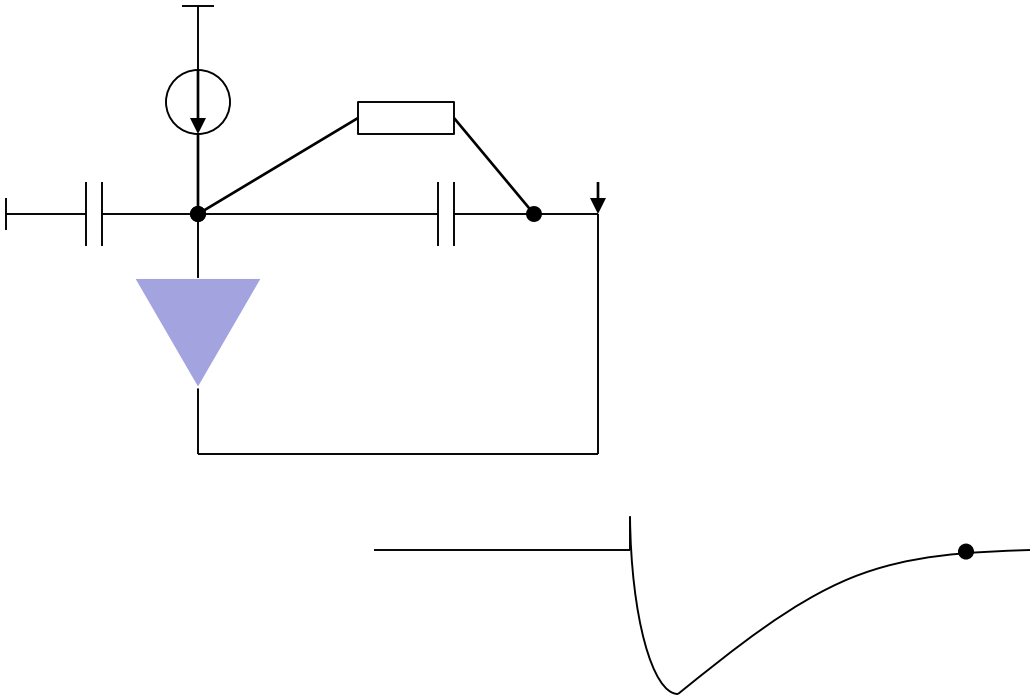



Q/C_f


Q/C_f

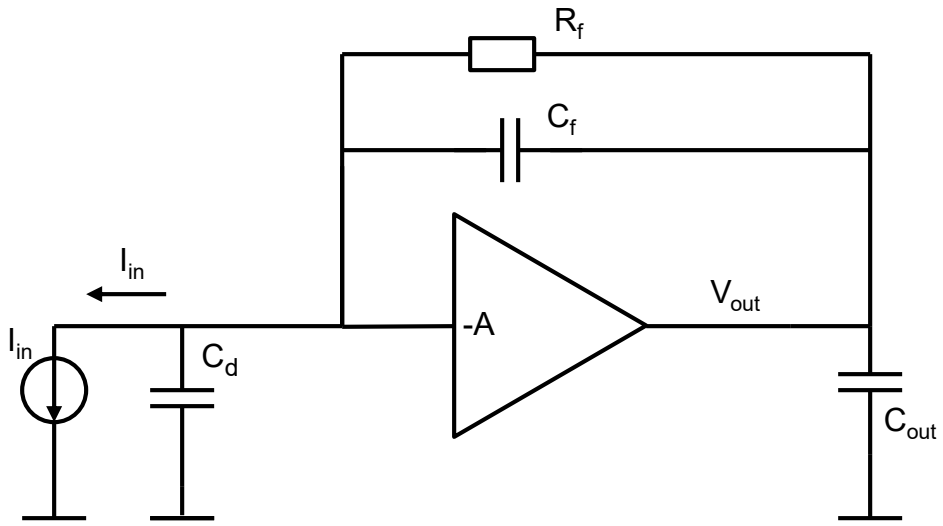

Q/C_f





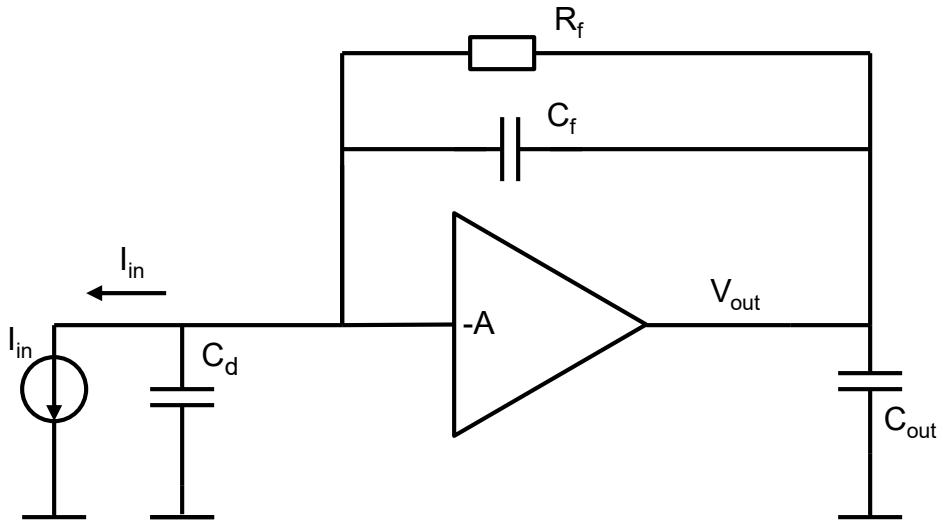
Charge sensitive amplifier - specifications

- Let us design CSA with the following specifications:
- Charge gain $V_{out,max}/Q_{in}$ = 1/2.5fF
- The detector capacitance is C_d = 100f
- The capacitive load is C_{out} = 1pF
- We want that the amplification depends only on C_f: $A_Q = \frac{V_{out,max}}{Q_{in}} = \frac{\alpha}{sC_f} \sim \frac{1}{C_f} = \frac{1}{2.5fF}$ (3). Therefore C_f = 2.5fF and $\alpha \sim 1$
- We specify T_f = 2.5µs
- Correct choice of T_r depends on the measurement we want to perform. If the aim is to measure amplitude, longer T_r is better (ideal for highest SNR is $T_r \sim T_f$)
- If time resolution should be optimized, the shortest possible T_r is better
- We specify $T_r \sim$ 50ns



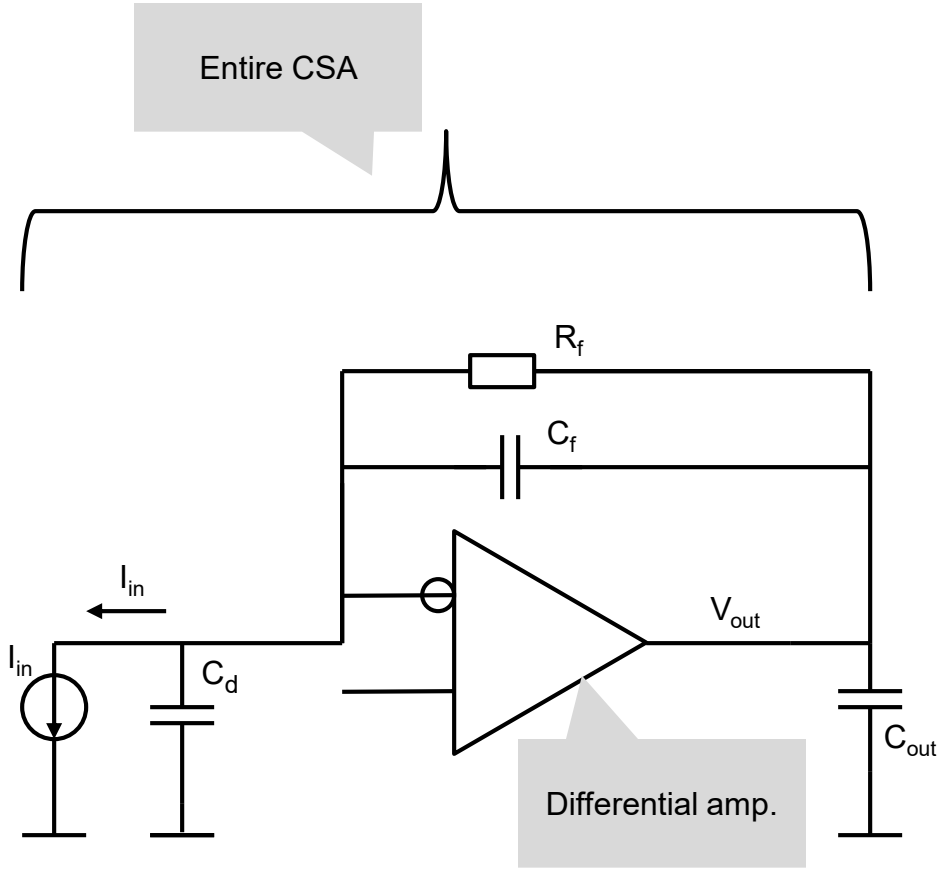
Amplification and T_f

- How large should be amplification A?
- To make amplification independent of other capacitances except C_f (specification (3)) factor $\alpha = \frac{\beta A}{1+\beta A}$ (2) should be nearly 1. Therefore it should hold βA >> 1. We chose βA = 10 (4)
- We will first calculate β: $\beta = \frac{C_f}{C_f + C_d} = \frac{2.5\text{fF}}{2.5\text{fF} + 100\text{fF}} \sim \frac{1}{40}$ (5)
- By substituting β = 1/40 into (5), we get A = 400
- How to achieve the specified time constants? Let us first take a look to T_f.
- For $\alpha \sim 1$, it holds $T_f = C_f R_f$
- We specified T_f = 2.5µs
- By substituting T_f = 2.5µs into the formula for T_f, we obtain R_f = 1GΩ



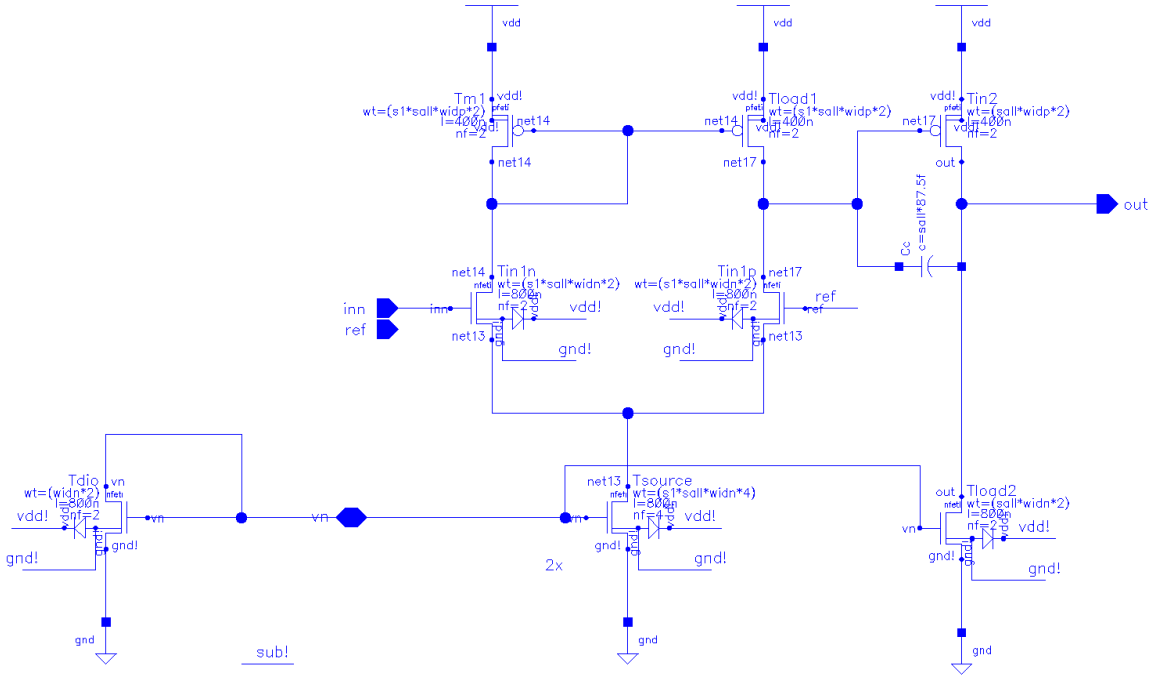
Amplifier choice

- Which amplifier type is suitable for the core part of the CSA?
- We chose differential amplifier for following reason:
- Differential amplifiers are less sensitive to noise and pickup in power lines – they have good power supply rejection ratio.
- We chose two-stage amplifier to achieve required open loop gain
- Such an amplifier is also called operational transconductance amplifier (OTA)



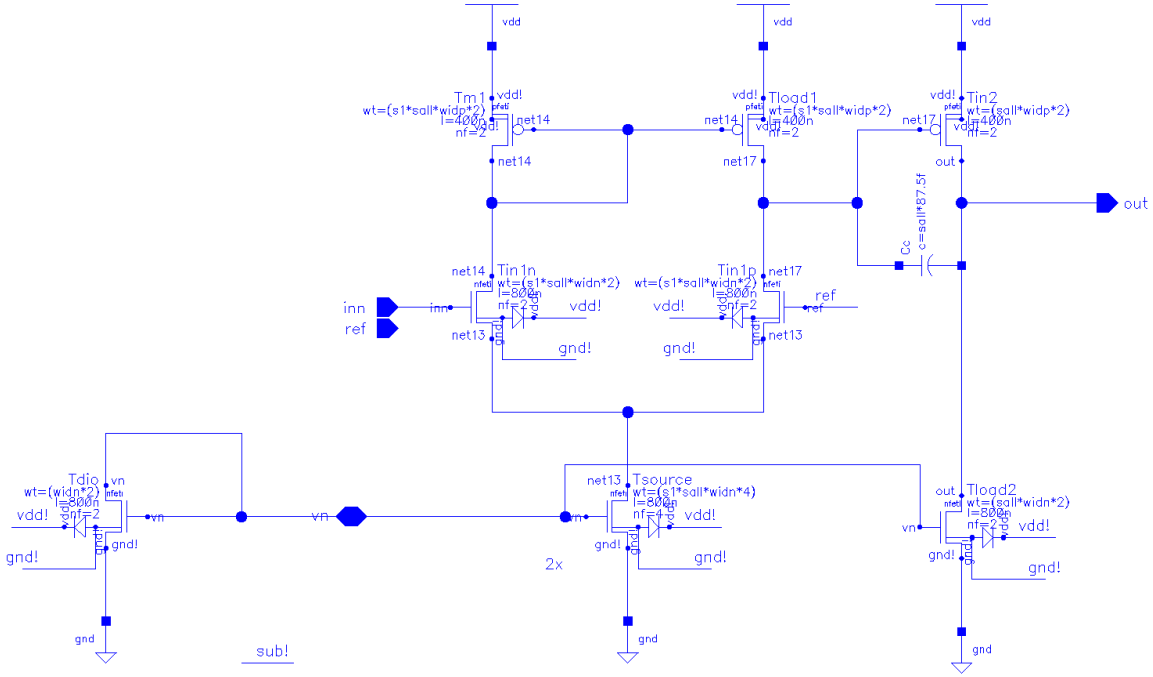
Two-stage differential amplifier

- The DC voltage gain of two stage operational transconductance amplifier (OTA) is:
- $A = A_1 \times A_2 = g_{m,in1}\, r_{out1}\, g_{m,in2}\, r_{out2}$ (6) with $r_{out1} = r_{ds,in1} \parallel r_{ds,load1}$; $r_{out2} = r_{ds,in2} \parallel r_{ds,load2}$
- If we substitute the simulated g_m and r_{ds} values ($g_{m,in1} \sim 70\mu S$, $g_{m,in2} \sim 50\mu S$, $r_{ds,pmos} = 800k\Omega$, $r_{ds,nmos} = 700k\Omega$) in (6), we obtain $A_1 \sim 25$, $A_2 \sim 20$ => $A \sim 500$
- DC gain is therefore large enough to assure $\alpha \sim 1$ (We obtain $\alpha \sim 0.93$, $\beta A = 12.5$)

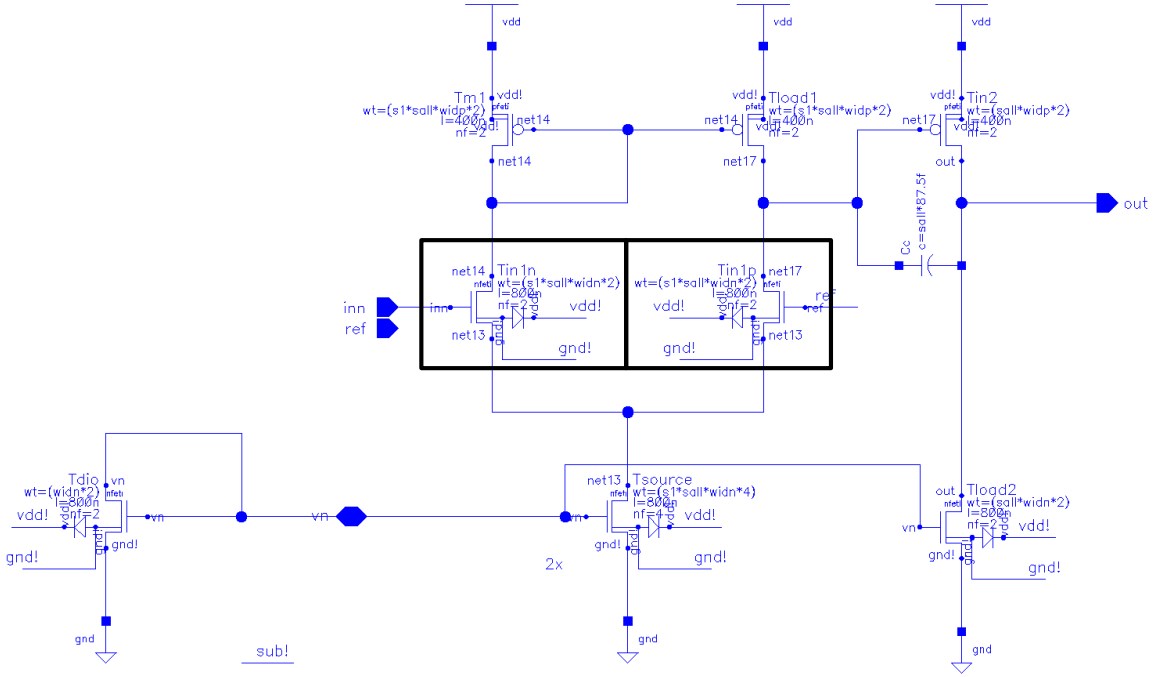


Two-stage differential amplifier

- The rise time constant of the pulse response of the two stage amplifier is:
- $T_r = C_c / (g_{m,in1}\ \beta)$; $\beta = C_f/(C_d+C_f)$ (7)
- If we chose $C_c = 87.5fF$, we obtain from (7) $T_r \sim 50ns$



- The performance of electronic systems is limited by noise. Without noise, an amplifier would be able to detect arbitrarily small inputs.
- The main noise sources are 1) the input transistors of OTA Tin1n and Tin1p with its flicker- and thermal noise, 2) shot noise of detector leakage current and 3) the resistor Rf (thermal noise)



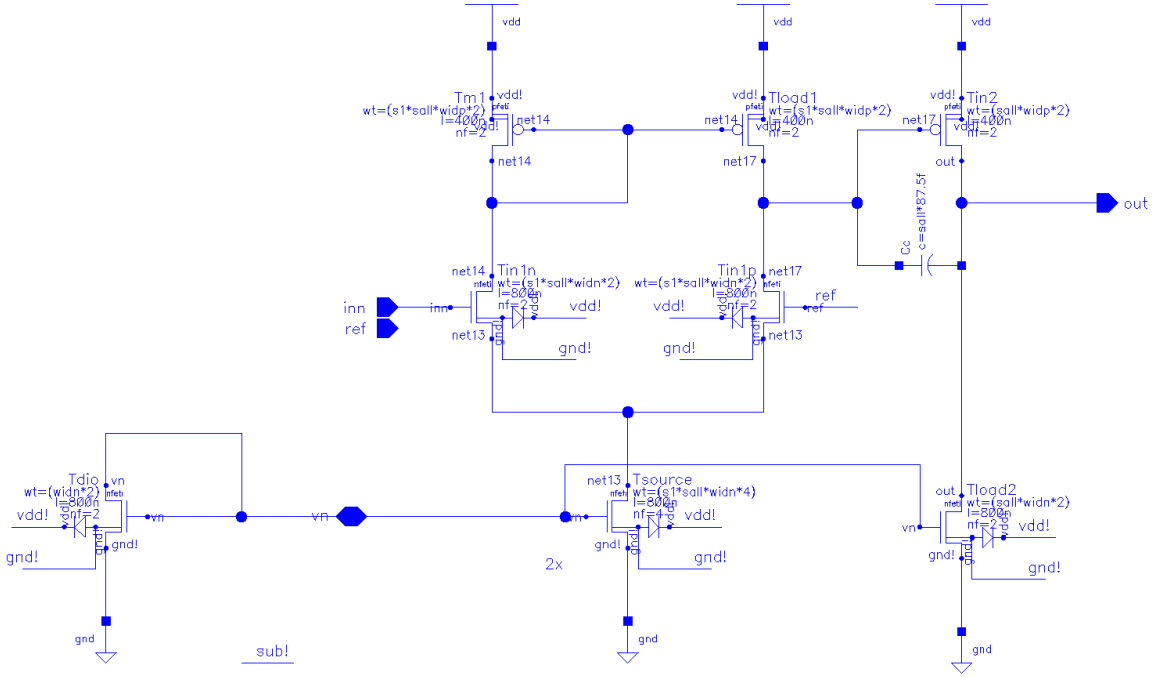
Noise - Theory

- The formula for equivalent noise charge (ENC[1]) is:
- $\mathrm{ENC}^2 = \frac{1}{4}\left(2 \times (\mathrm{C_{det}} + \mathrm{C_f})^2 \left(\mathrm{m\,k_f} + \frac{\mathrm{S_{VT}}}{\mathrm{T_r}}\right) + \mathrm{S_{ID}\,T_f} + \mathrm{S_{IR}\,T_f}\right)$ (8)
- The parameters are:
- $\mathrm{S_{VT}}$ is the power spectral density (PSD) for thermal noise of each input transistor. $\mathrm{S_{VT}} = \frac{4\mathrm{kTn}2/3}{\mathrm{g_m}}$; with k Boltzmann constant, T absolute temperature and slope factor n ~ 1.25.
- $\mathrm{S_{ID}}$ is PSD of shot noise of detector leakage current I_{leak}: $\mathrm{S_{ID}} = 2\mathrm{eI_{leak}}$
- $\mathrm{S_{IR}}$ is PSD of thermal noise of R_f: $\mathrm{S_{IR}} = \frac{4\mathrm{kT}}{\mathrm{R_f}}$
- $\mathrm{k_f}$ is coefficient of flicker noise for each input transistor. Power spectral density of flicker noise is k_f/f
- It can be derived: $\mathrm{k_f} = \frac{\mu \mathrm{e}^2 \langle \mathrm{n_{it}} \rangle \mathrm{I_{dssat}}}{\mathrm{L}^2 \mathrm{n C'_{ox} g_m^2}}$; with n_{it} density of traps that generate noise. Factor m is nearly $4 \times \frac{\mathrm{t_{peak}}}{\mathrm{T_r}} \sim 16$
- Notice factor “2 ×” in eq. (8) because there are two input transistors, whose noise power adds
- Questions:
- Which noise component gets large for fast amplifier (T_r small)?
- Which noise components get smaller when we increase the widths and currents of all transistors, without changing T_r?

1: ENC is the input signal that produces the output amplitude equal to root mean square (RMS) of noise

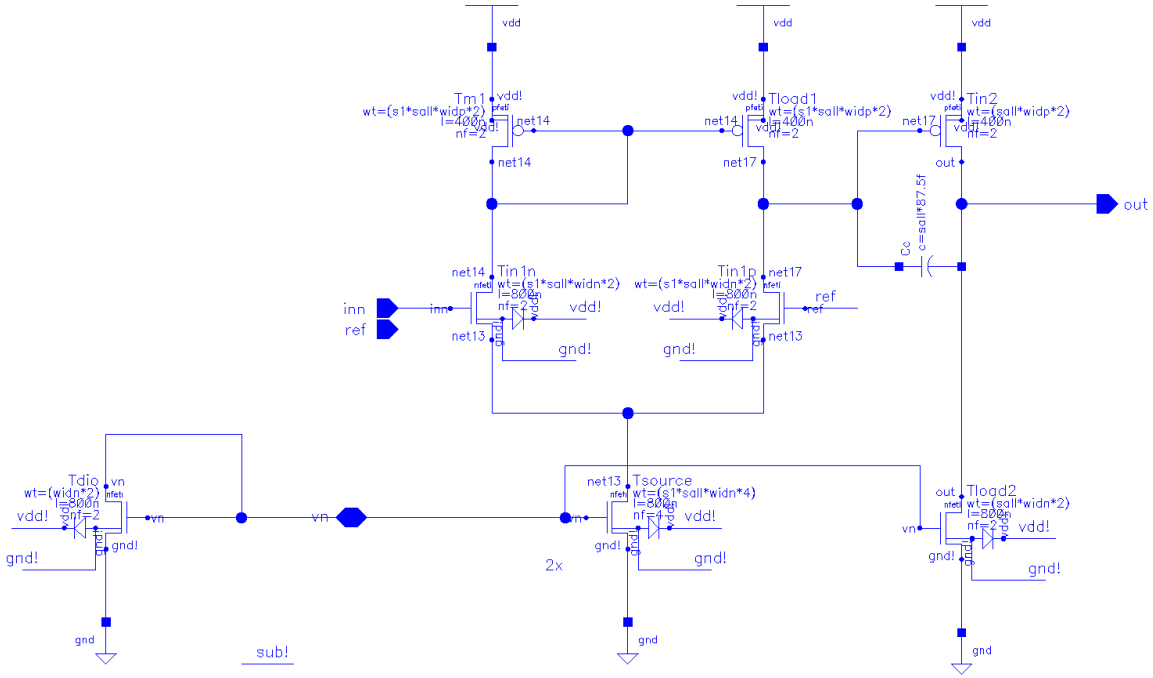
An optimization method for low noise

- We have fulfilled the specifications for current, gain and time constant. Let us now optimize the amplifier to have lowest possible noise.
- To optimize the amplifier, we could 1) scale up the transistor widths in the first stage (parameter s1), 2) scale up the widths in the second stage, 3) scale up C_c and 4) scale up all transistor widths and C_c (parameter sall)



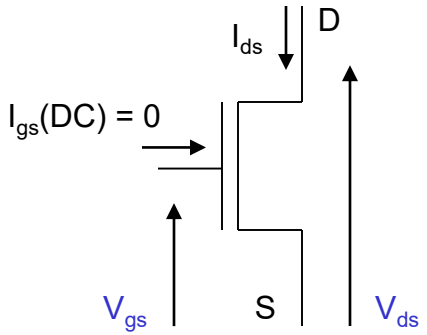
An optimization method for low noise

- By scaling up first stage, amplifier gets faster, without affecting noise
- By scaling down C_c amplifier gets faster and noise increases, amplifier may get instable
- Scaling up of second stage makes amplifier more stabile
- Scaling up all parameters improves noise, however current consumption increases
- We introduced scaling factors s1 and sall to allow optimization of the circuit



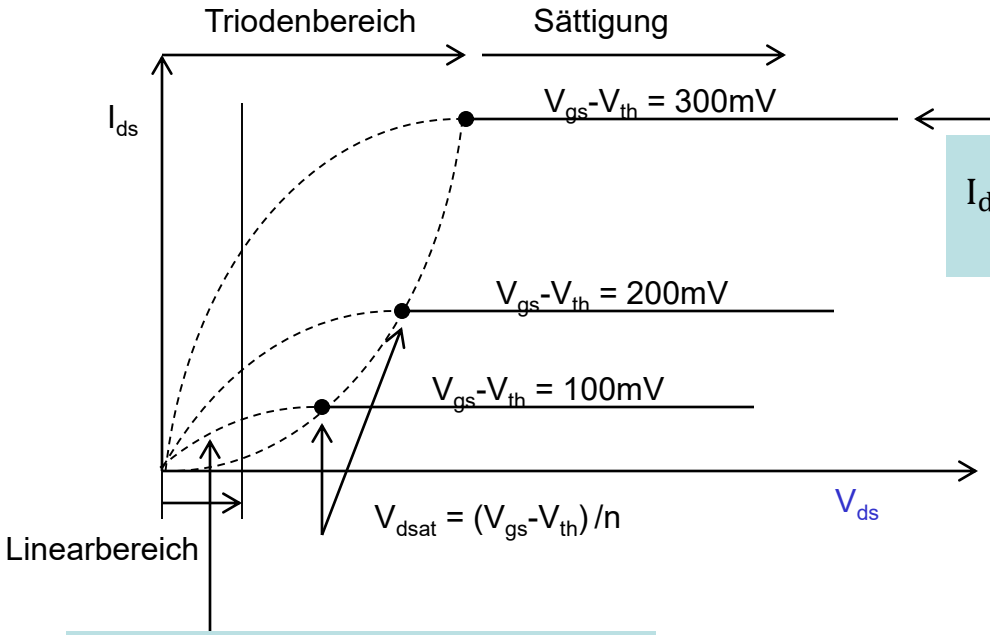
MOSFET
Metal oxide semiconductor field effect transistor

- The state of the transistor is described by two voltages – V_{gs} and V_{ds} and by two currents I_{ds} and I_{gs}.
- Gate represents only a capacitance, no DC current flows



I_{ds} (V_{ds}) Characteristic

- I_{ds}-V_{ds} characteristics for different V_{gs} – e.g. 100mV, 200mV...
- In the right line region, the current is relatively independent of V_{ds} – we call it the saturation region
- Ideally: $I_{ds} = I_{dssat}$ for all $V_{ds} > V_{dssat}$
- In the left line region, the current drops to 0. We call this region the triode range. For small Vds, the current-voltage dependence is approximately linear (linear range)

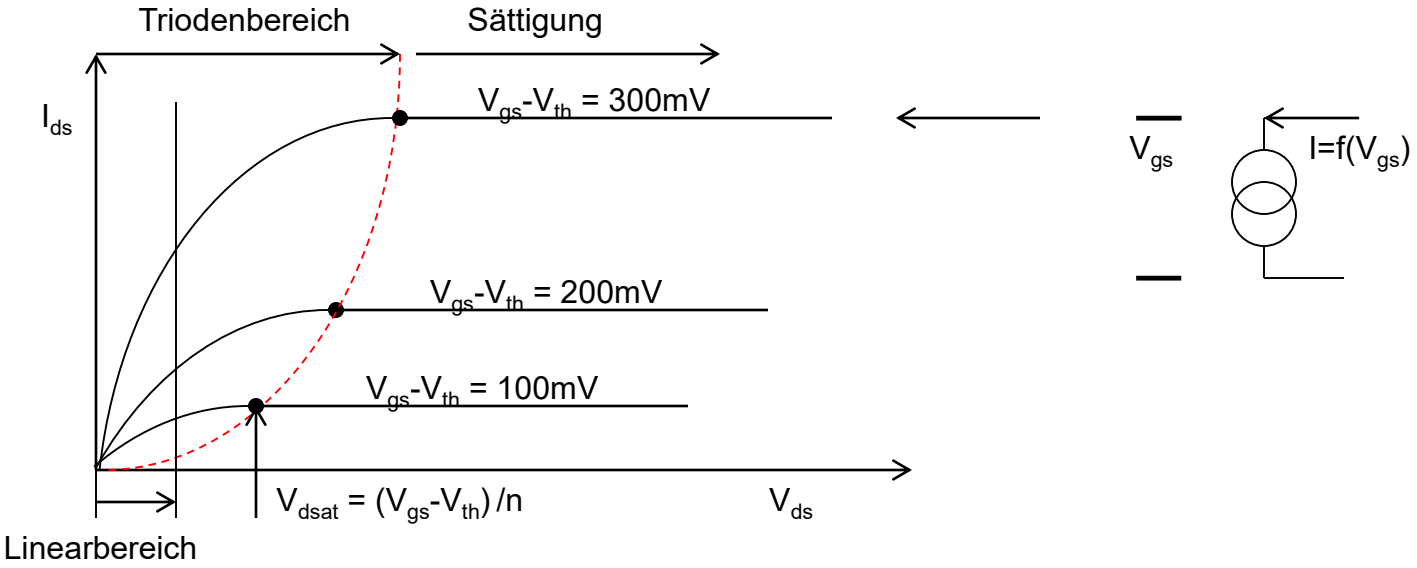


$$I_{dssat} = \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{thsb})^2$$

$$I_{ds} = \mu C'_{ox}\frac{W}{L}(V_{gs} - V_{thsb})V_{ds}$$

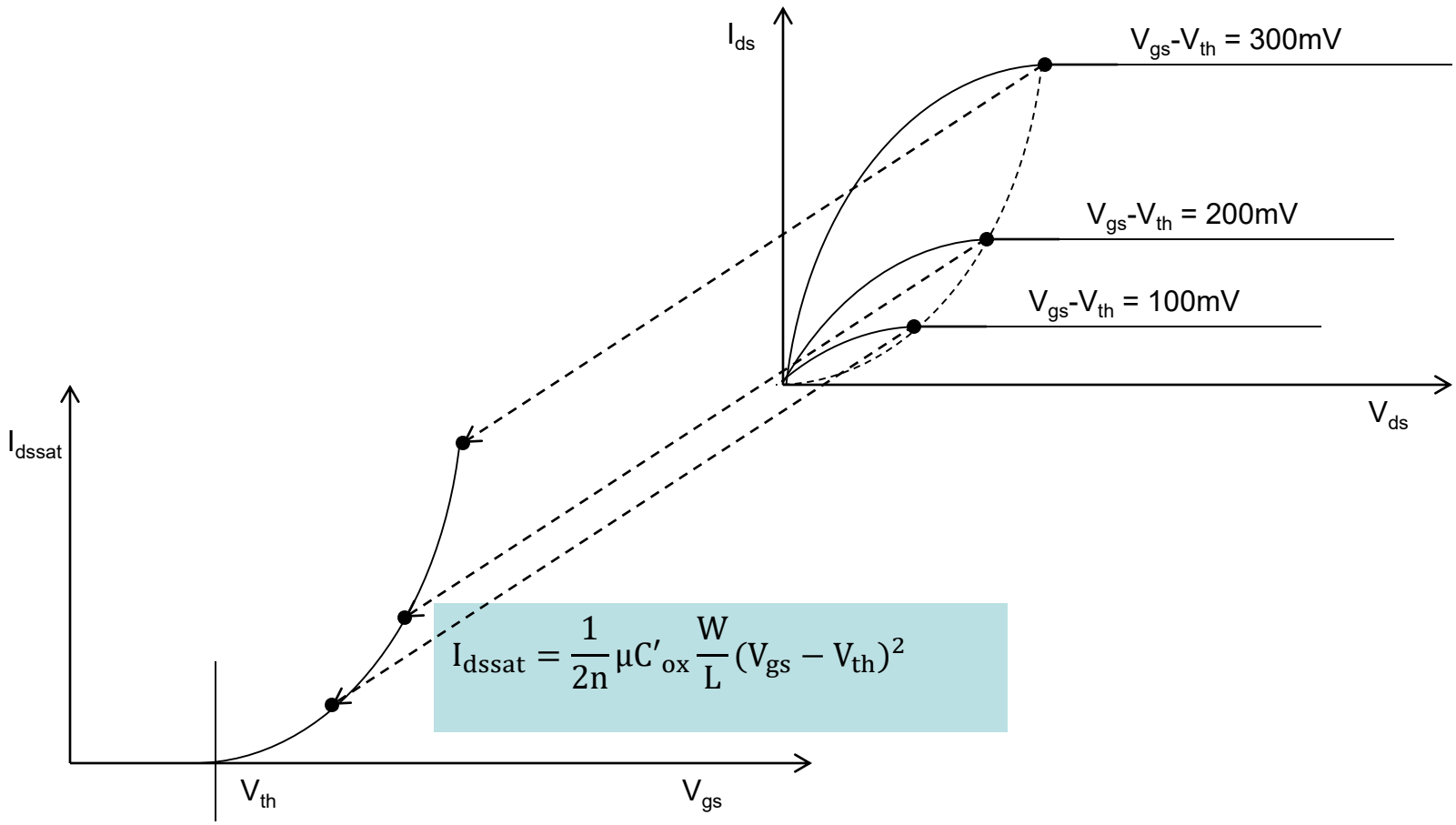
I_{ds} (V_{ds}) Characteristic - Saturation

- Current in saturation depends quadratically on Vgs
- $I_{dssat} = \frac{1}{2n} \mu C'_{ox} \frac{W}{L} (V_{gs} - V_{thsb})^2$
- At the boundary between the saturation and triode region holds: $V_{ds} = V_{dssat} = (V_{ds}-V_{thsb})/n$
- In the saturation range, the transistor behaves like a voltage-controlled current source



I_{dssat} (V_{gs}) Characteristic

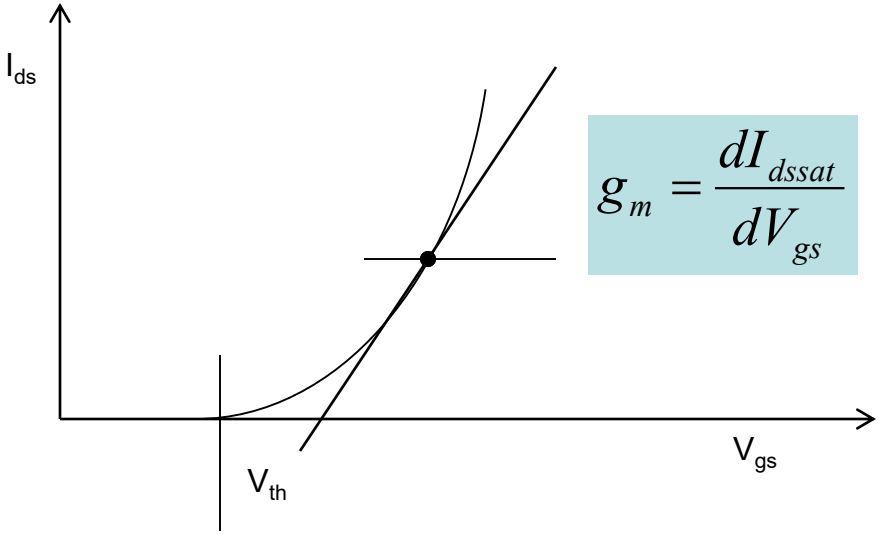
- I_{ds}-V_{gs} characteristic



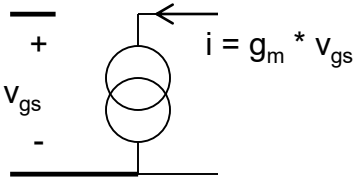
$$I_{dssat} = \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{th})^2$$

g_m - Transconductance

- The input characteristic is linearized in the area around the operating point -> small signal model
- The slope of the line $g_m = dI_{dsat}/dV_{gs}$ is called transconductance.
- For the small signals, the linear models are used



$$g_m = \frac{dI_{dssat}}{dV_{gs}}$$



$$g_m = \frac{dI_{dssat}}{dV_{gs}}$$

$$I_{dssat} = \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{gs} - V_{thsb})^2$$

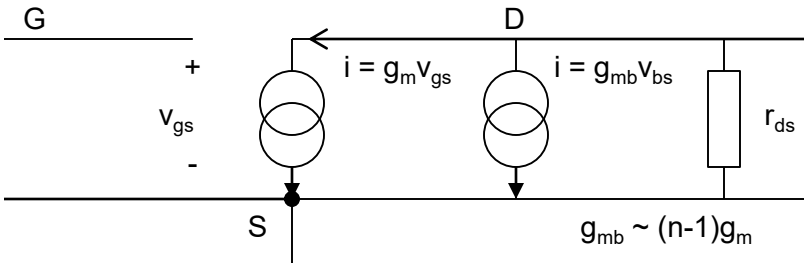
$$I_{dssat} = \frac{k}{2}\frac{W}{L}(V_{gs} - V_{thsb})^2$$

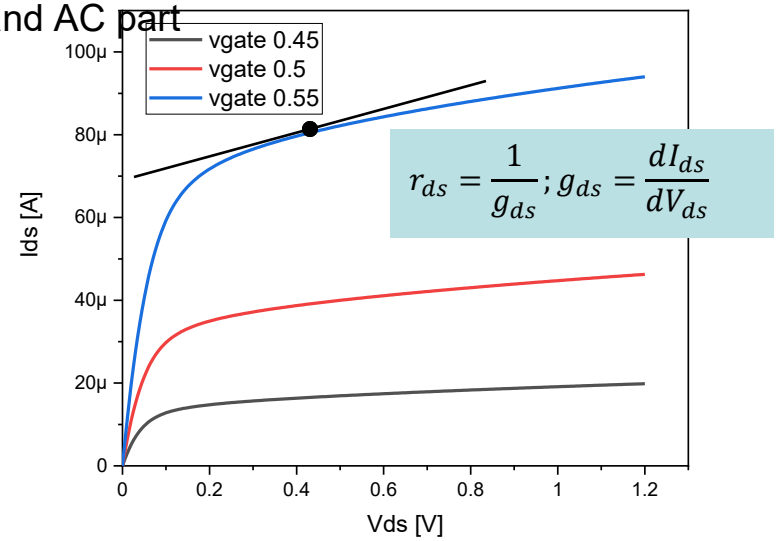
$$g_m = \sqrt{2kI_{dssat} \cdot (W/L)}$$

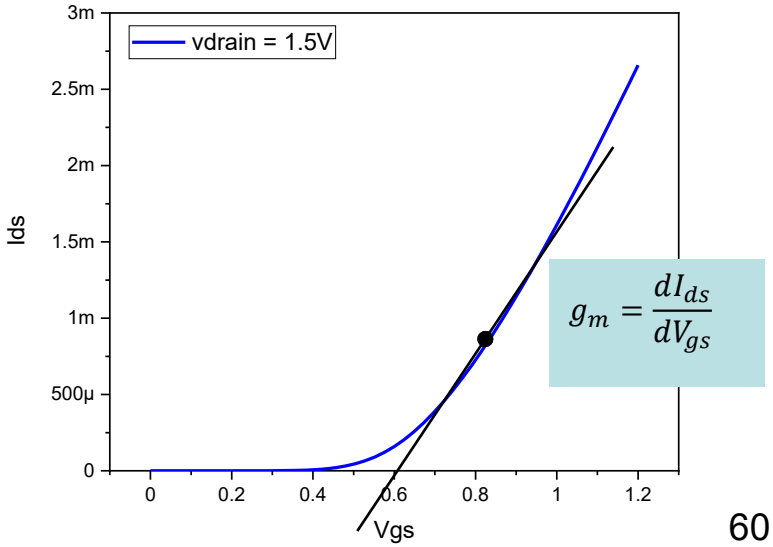
Small signal model

Small signal model

- $I_{ds} = I_{dssat}(V_{gst})\left(1 + \frac{V_{ds} - V_{dssat}}{V_A}\right); v_{gst} = V_{gs} - V_{thsb}; V_{thsb} = V_{th} - (n-1)V_{bs}$
- $V_{dssat} = (V_{ds} - V_{thsb})/n$
- Small signal. The equation ca be decomposed into DC and AC part
- $i_{DS} = I_{ds,DC} + i_{ds,ac}$
- $i_{ds,ac} = \frac{dI_{ds}}{dV_{gs}} v_{gs} + \frac{dI_{ds}}{dV_{ds}} v_{ds} + \frac{dI_{ds}}{dV_{sb}} v_{bs}$
- $= g_m v_{gs} + g_{ds} v_{ds} + g_{mb} v_{bs}$





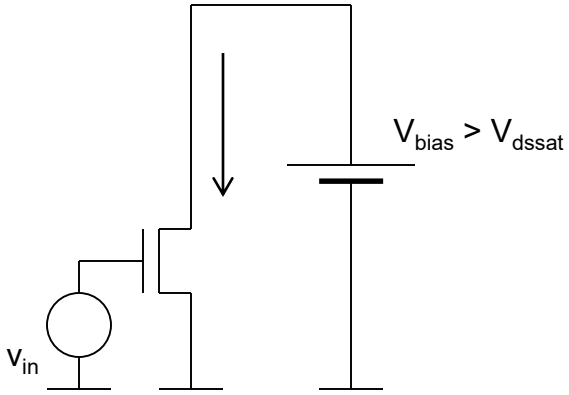


Basic analog circuits

Basic analog circuits
Current source

Voltage-controlled current source

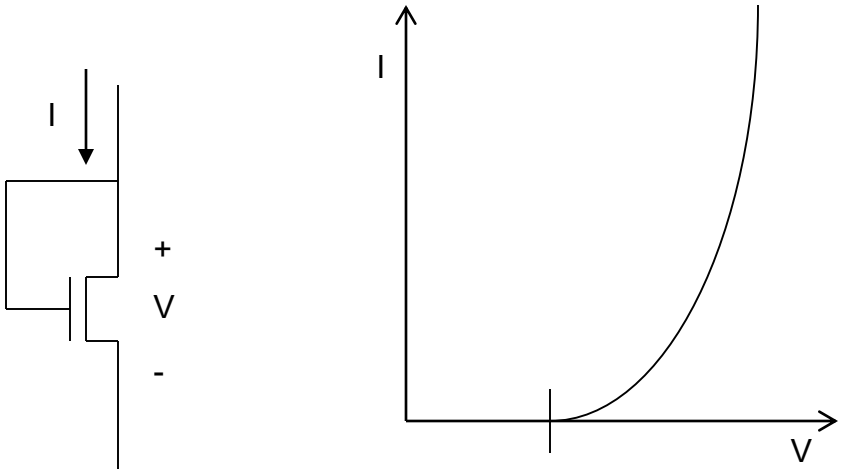
- Voltage-controlled current source (U-I converter)
- Signal voltage is at the gate
- Drain is connected to bias voltage to assure transistor saturation. Condition: $V_{ds} > V_{dssat}$
- It holds
- $I_{out} = \frac{1}{2n}\mu C'_{ox}\frac{W}{L}(V_{in} - V_{thsb})^2$; n is the slope factor n ~ 1.25; V_{thsb} is the threshold voltage $V_{thsb} = 0.5V + (n-1)\,V_{sb}$



Basic analog circuits
Diode-connected transistor

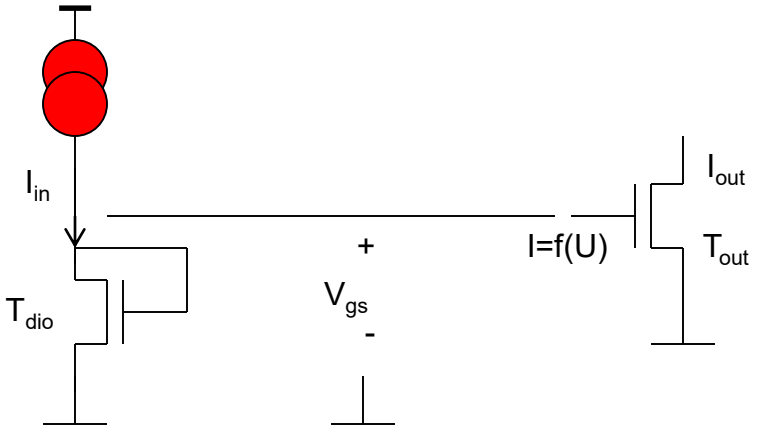
Diode-connected transistor

- $V_{ds} = V_{gs} > \frac{V_{gs} - V_{thsb}}{n} \equiv V_{dssat}$
- deshalb
- $I_{ds} = I_{dssat}$
- $I_{dssat} = \frac{1}{2n} \mu C'_{ox} \frac{W}{L} (V_{gs} - V_{thsb})^2$



Basic analog circuits
Current mirror

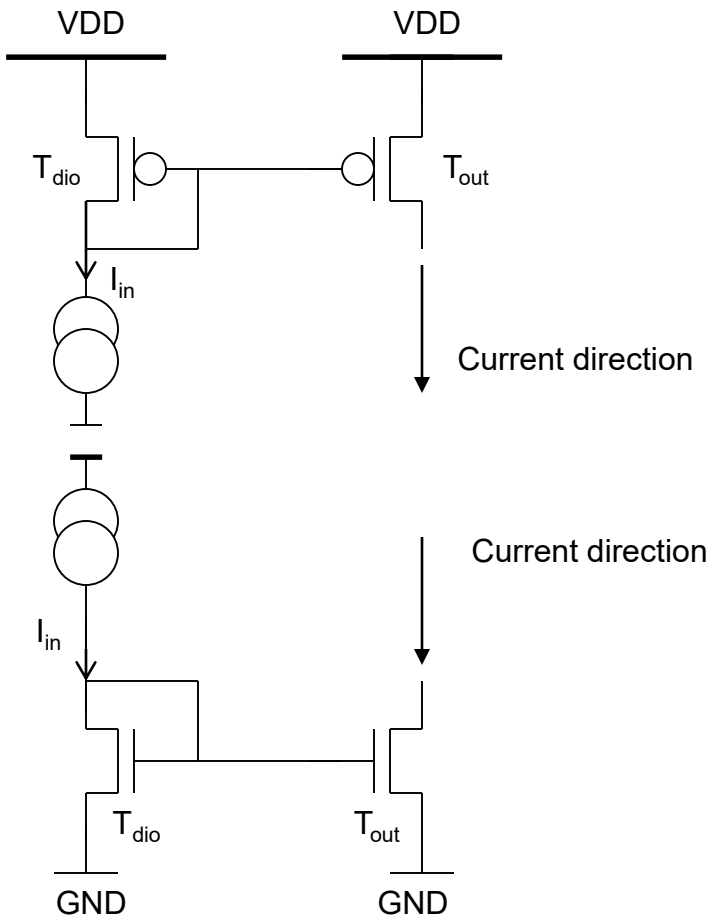
- A current mirror is the combination of a MOSFET diode and a current source
- $I_{in} = k_s \frac{W_{dio}}{L_{dio}} (V_{gsdio} - V_{th})^2 (1 + \frac{V_{dsdio} - V_{dssat}(V_{gsdio})}{V_A})$
- $V_{dsdio} = V_{gsdio} = V_{in}$ (diode short)
- $I_{out} = k_s \frac{W_{out}}{L_{out}} (V_{gsout} - V_{th})^2 \left(1 + \frac{V_{dsout} - V_{dssat}(V_{gsout})}{V_A}\right)$
- $V_{gsdio} = V_{gsout} = V_{in}$ (gate connection); $V_{dsout} = V_{out}$ (definition)
- Condition1: T_{out} in saturation and
- Condition 2: $V_A \gg V_{ds} - V_{dssat}$ or $V_{in} \sim V_{out}$



$$\frac{I_{out} = k_s \frac{W_{out}}{L_{out}} (V_{in} - V_{th})^2}{I_{in} = k_s \frac{W_{dio}}{L_{dio}} (V_{in} - V_{th})^2}$$

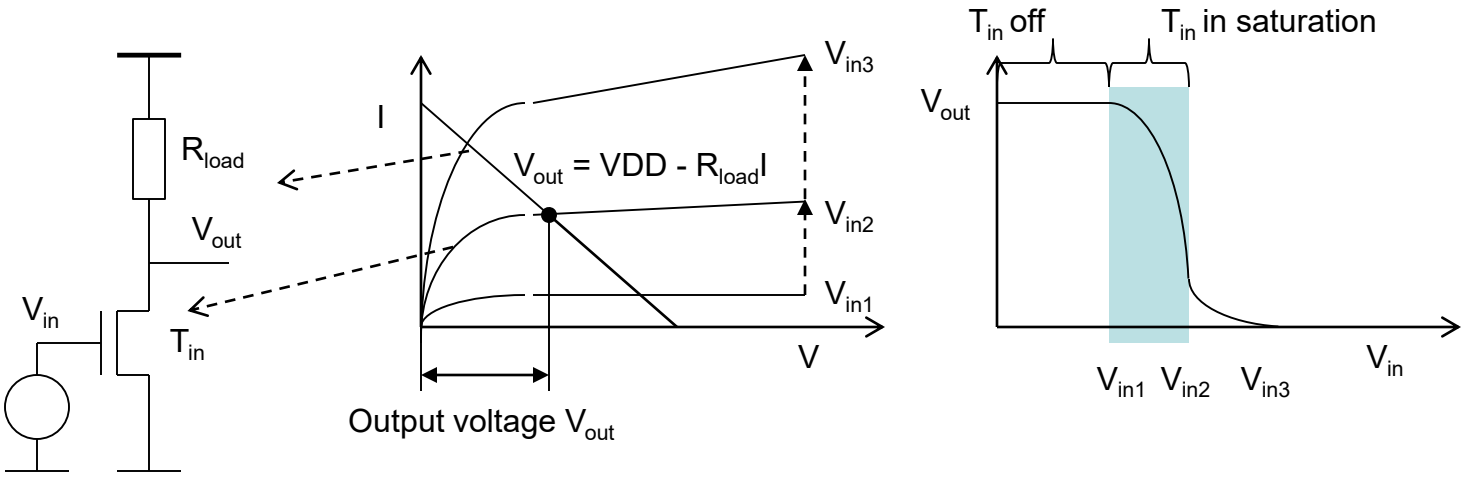
$$I_{out} = I_{in} \frac{\left(\frac{W_{out}}{L_{out}}\right)}{\left(\frac{W_{dio}}{L_{dio}}\right)}$$

- PMOS current mirror: Source connected to VDD (positive power supply), current flows "to the outside"
- NMOS current mirror: Source connected to GND, current direction inwards

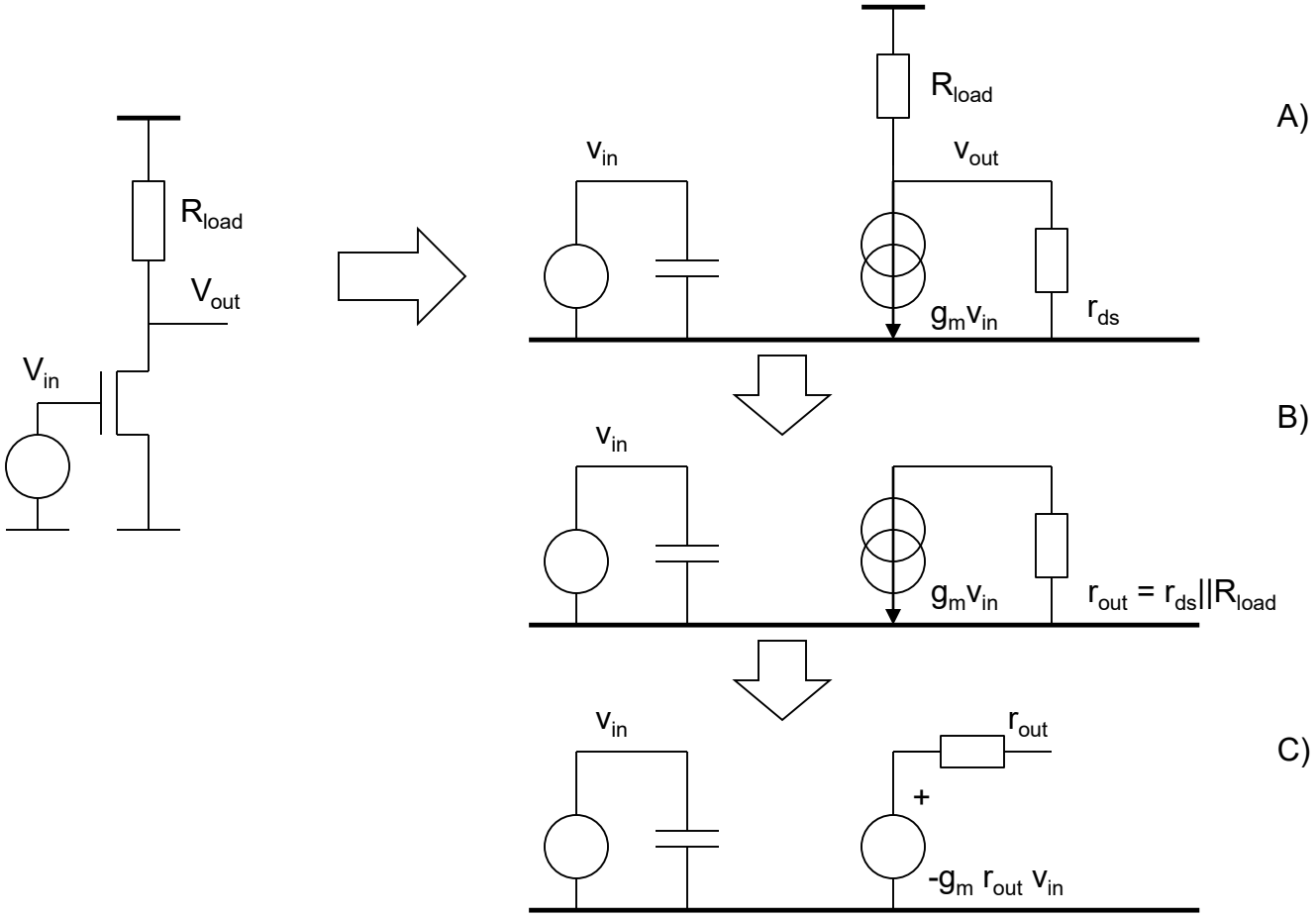


Basic analog circuits
Common source amplifier with resistor

- We can derive the characteristic curve mathematically (with the help of equations) or graphically (with the help of characteristic curves).
- Load line analysis



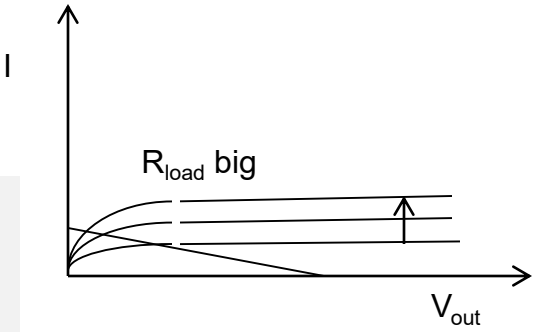
- For the working area where Tin is in saturation (condition is $V_{out} > V_{dssat} = V_{in} - V_{th}$), we can draw the small signal circuit.
- The voltage amplification is :
- $A = v_{out}/v_{in} = -g_m (r_{ds} \,||\, R_{load})$



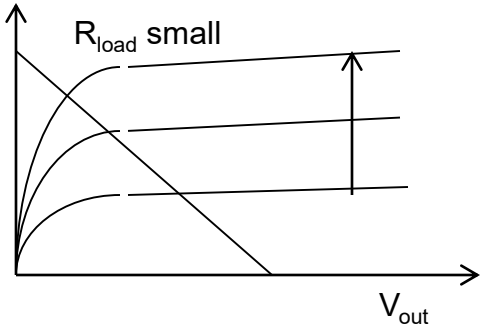
Basic analog circuits
Common source amplifier with active load

- To maximize amplification, we need relatively large values for g_m and r_{out}.
- The disadvantage of the amplifier with a linear resistor is that you cannot maximize both g_m and $r_{out} = R_{load} \parallel r_{ds}$.
- Why?
- $r_{ds} = \frac{E_{sat} L}{I_{dssat}}$
- $g_m \sim I_{dssat}$

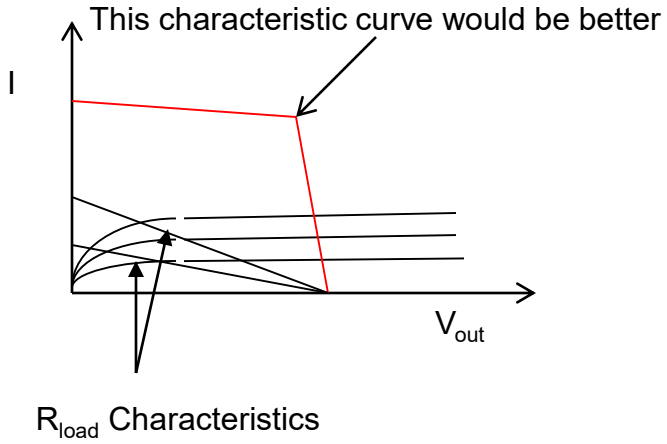
If the resistance R_{load} is large, its characteristic curve is close to the X-axis. The transistor current is then small. A small current leads to a small transconductance



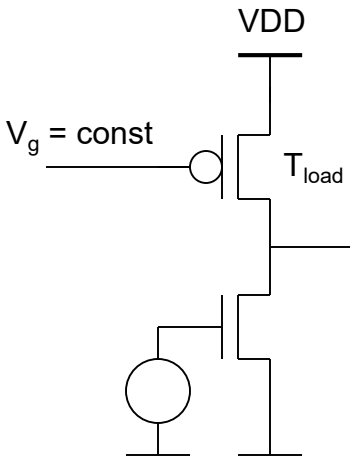
If R_{load} is small, the characteristic curve increases. The transistor current and gm are higher. However, because of the small R_{load}, the gain is small.

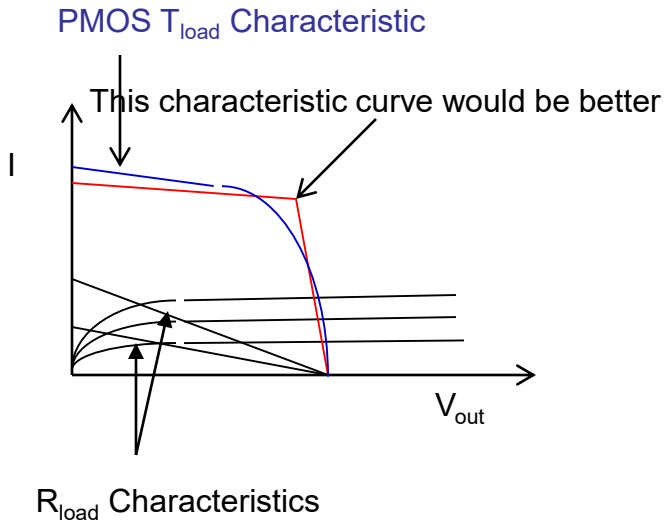


- A load characteristic curve that rises relatively quickly and then runs horizontally in the large area would be better than the characteristic curve of linear resistor.



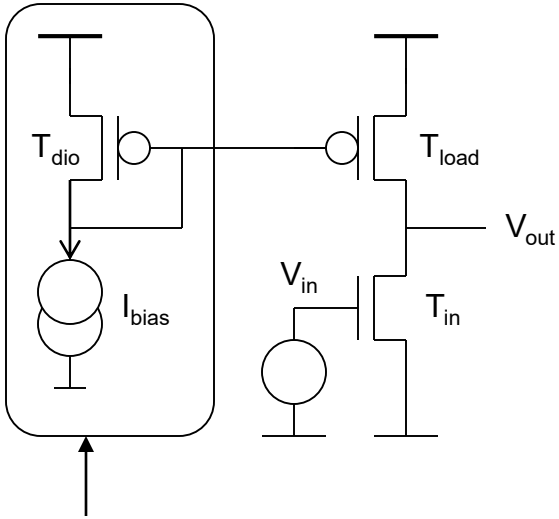
- A PMOS current source has an almost ideal characteristic curve





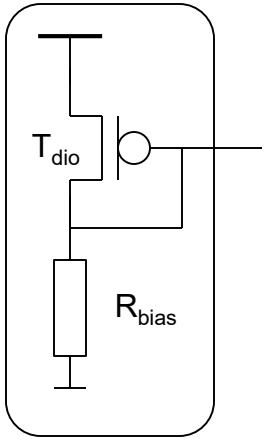
- We get a better amplifier when we replace resistor R_{load} with a PMOS current source
- A load element realized with a transistor is called active load

Bias circuit



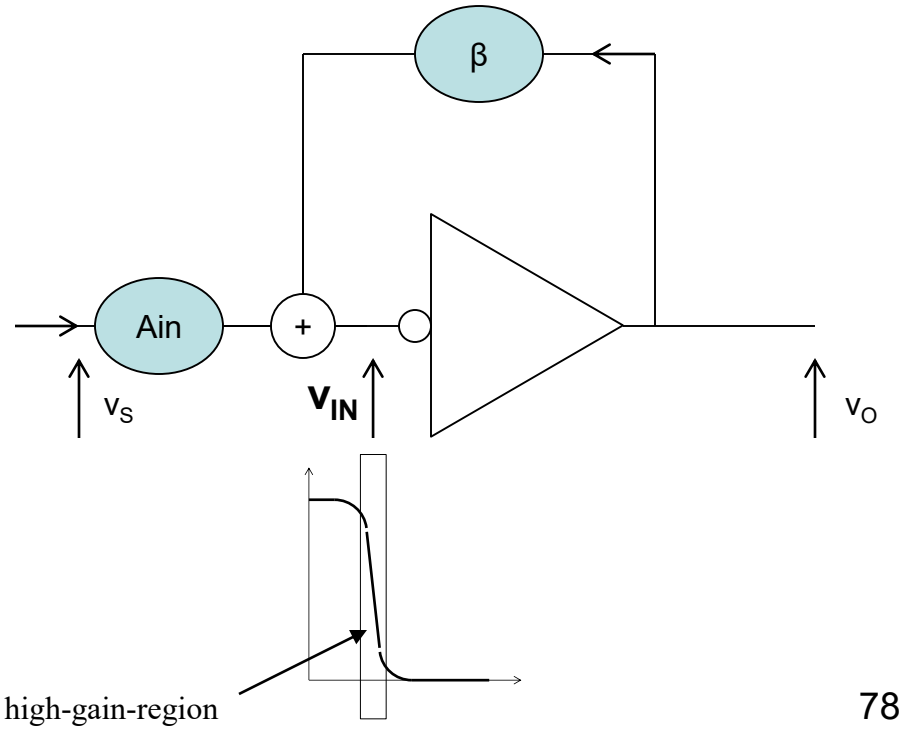
Bias circuit for the current source in the form of MOSFET diode and a current source.

Simple implementation of the bias circuit



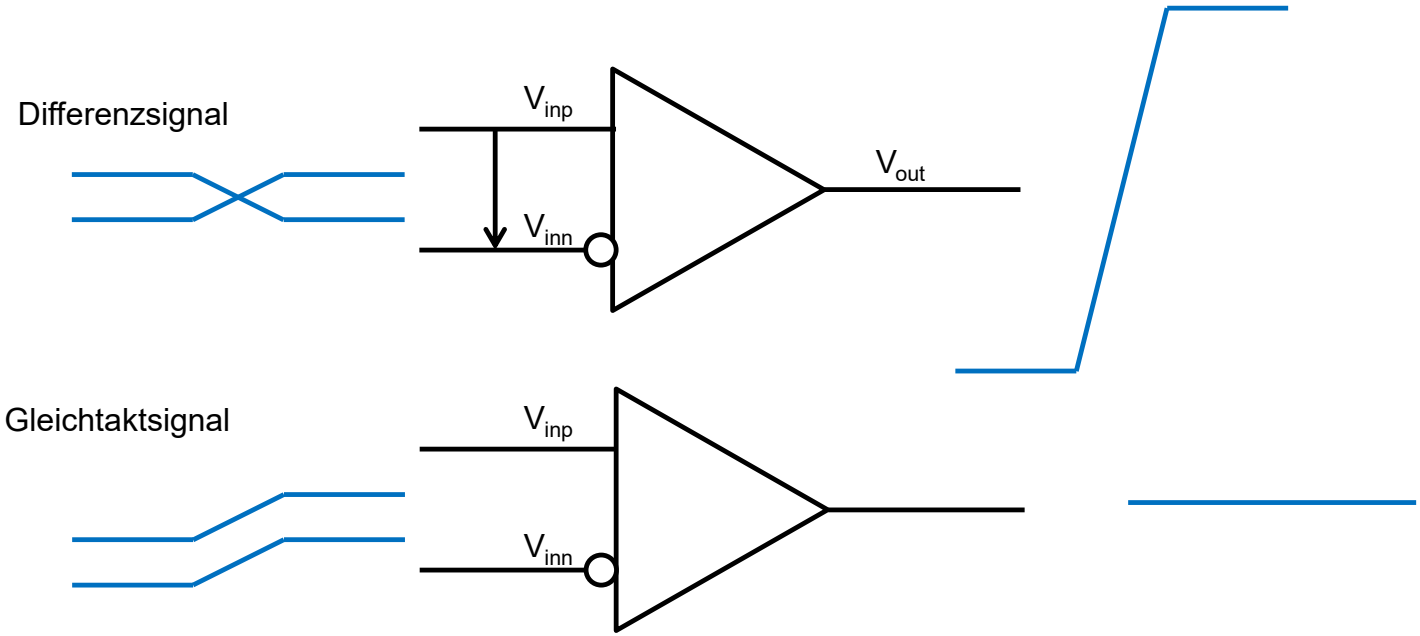
Feedback

- An important technique that turns the non-ideal active components into good linear amplifiers is negative feedback. Feedback enables the design of precise amplifiers and oscillators
- Feedback: Automatic regulation of the voltage v_{IN} to the “threshold”
- FB allows, in addition to control, also signal amplification
- $v_{IN} = A_{IN} v_S + \beta v_O$
- v_{IN} = const (Regelung)
- $dv_O = \frac{-A_{IN}}{\beta} dv_S \equiv dv_S \, AFB$



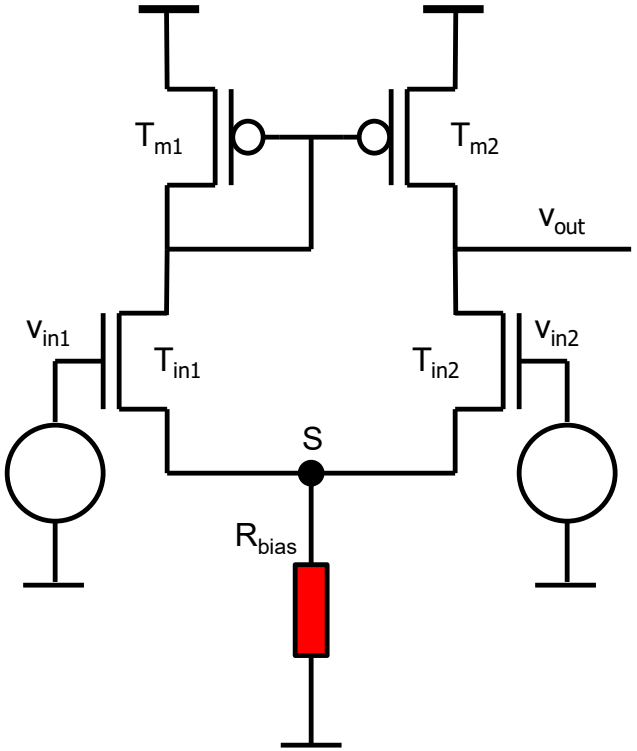
Differential amplifier

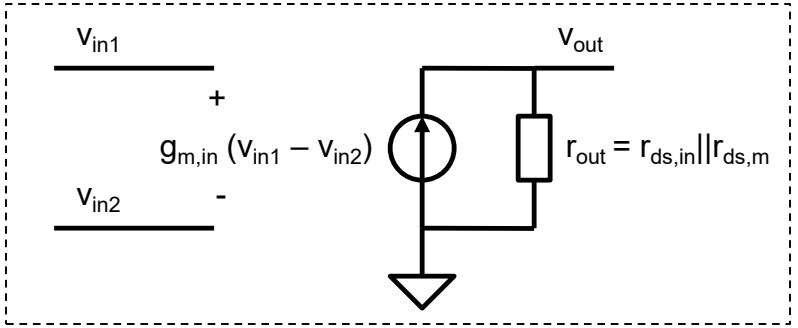
- Differential amplifiers



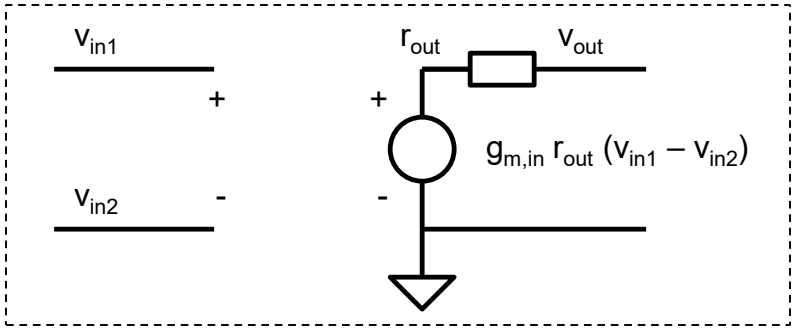
Differential amplifier small signal model

- Differential amplifiers



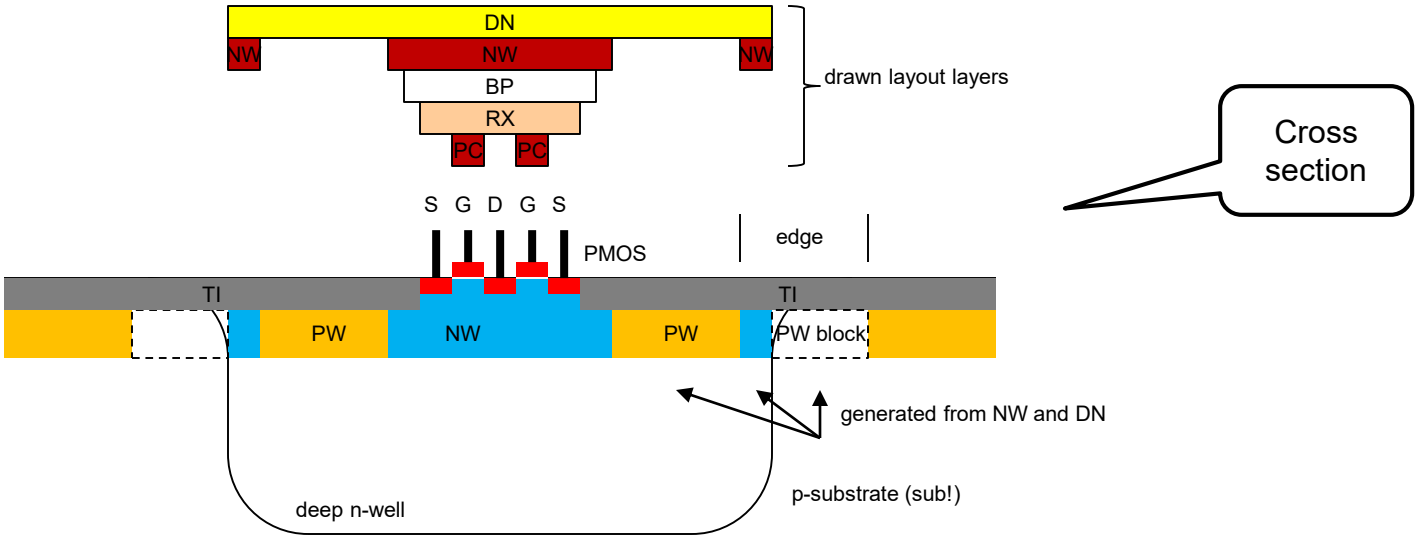


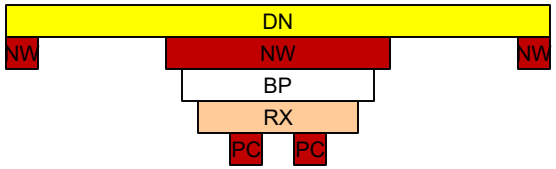
Small signal model with a current source



Small signal model with a voltage source

Layout

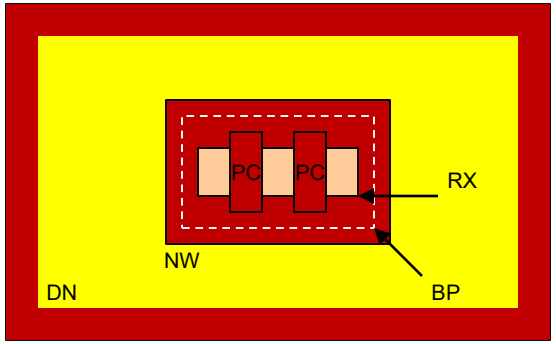

DN
NW
NW
NW
BP
RX
PC
PC
drawn layout layers
Cross section
S G D G S
PMOS
edge
TI
TI
PW
NW
PW
PW block
generated from NW and DN
deep n-well
p-substrate (sub!)



drawn layout layers

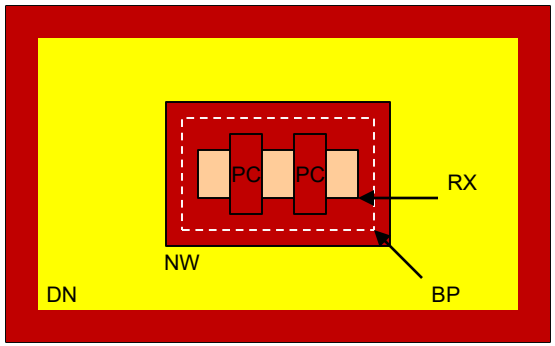
Cross section

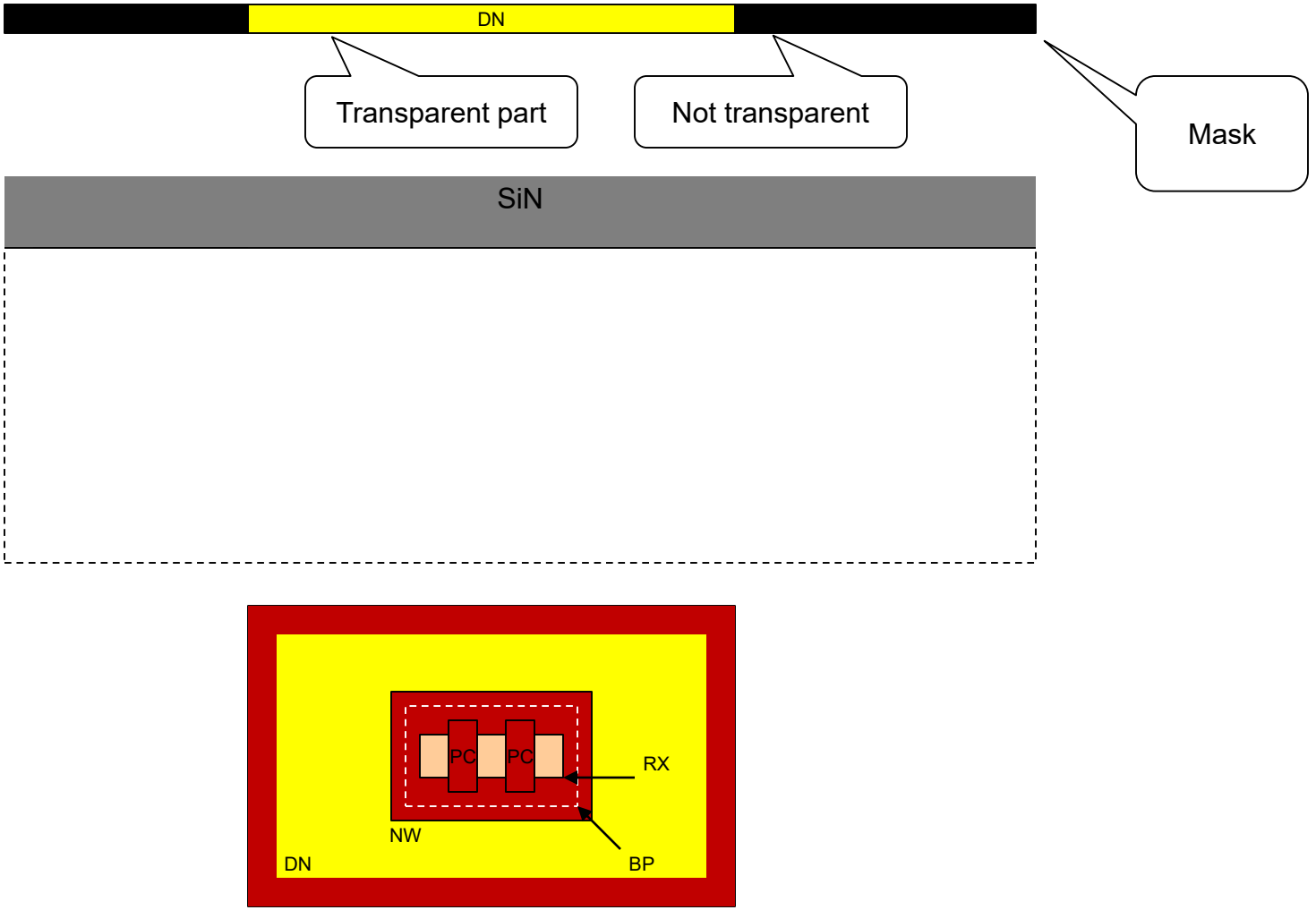
Si substrate Cross section

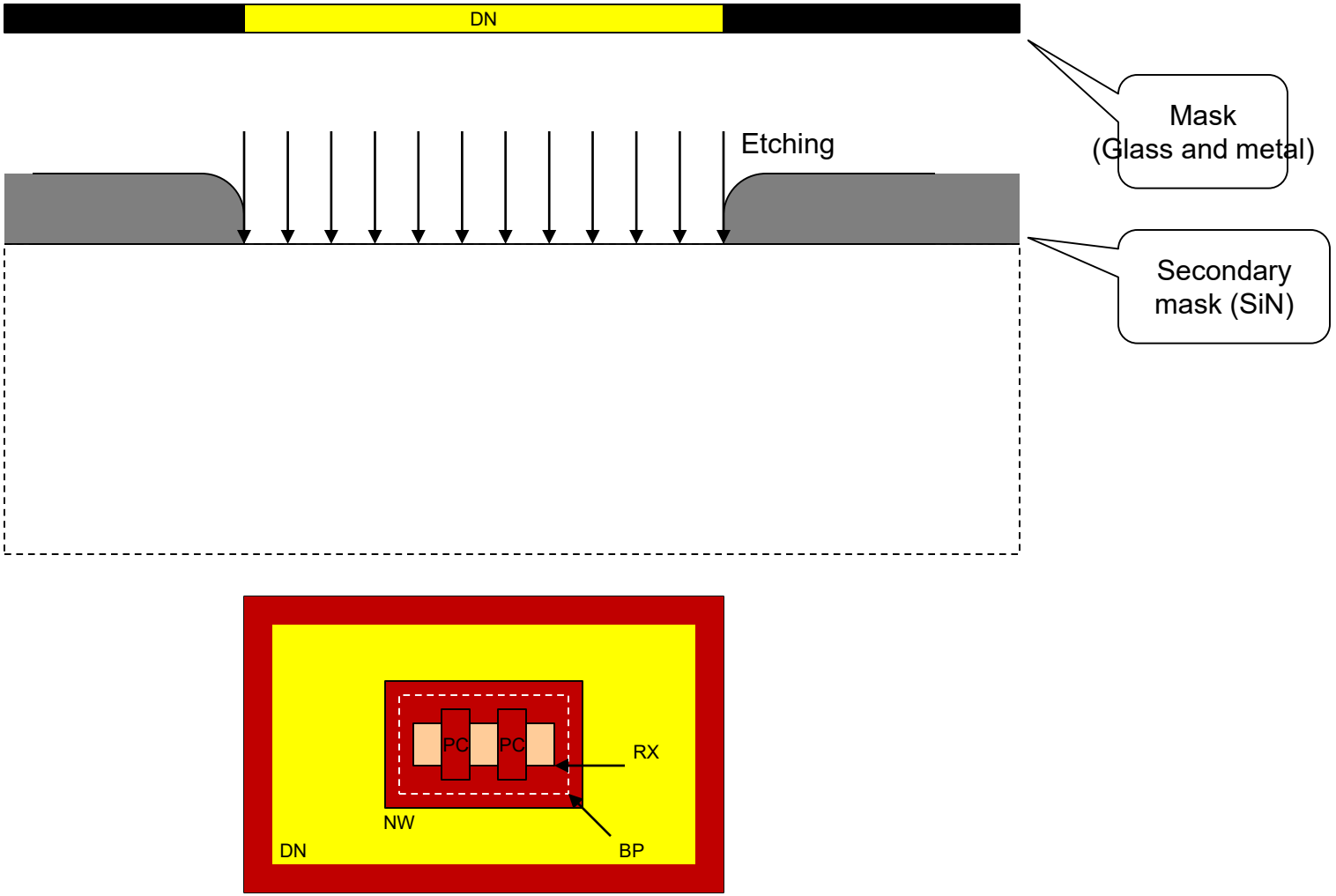


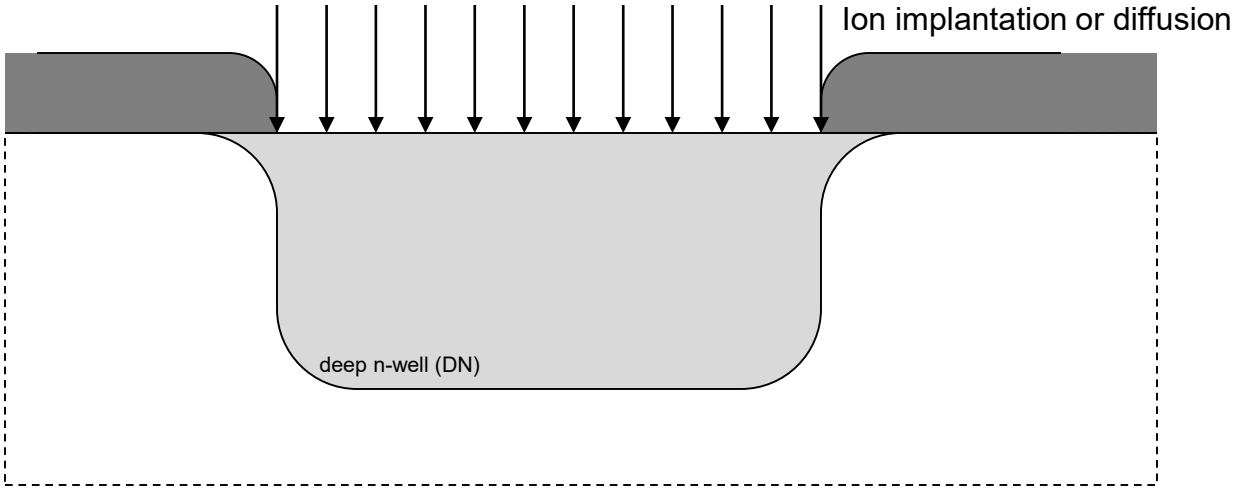
Top view

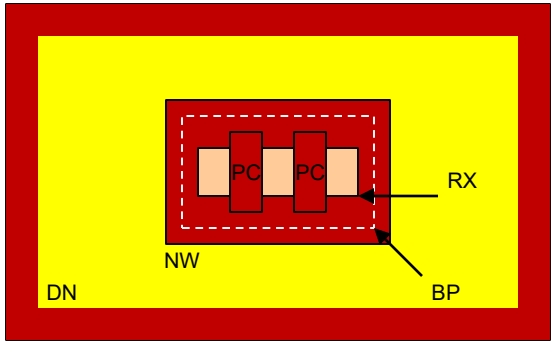
SiN

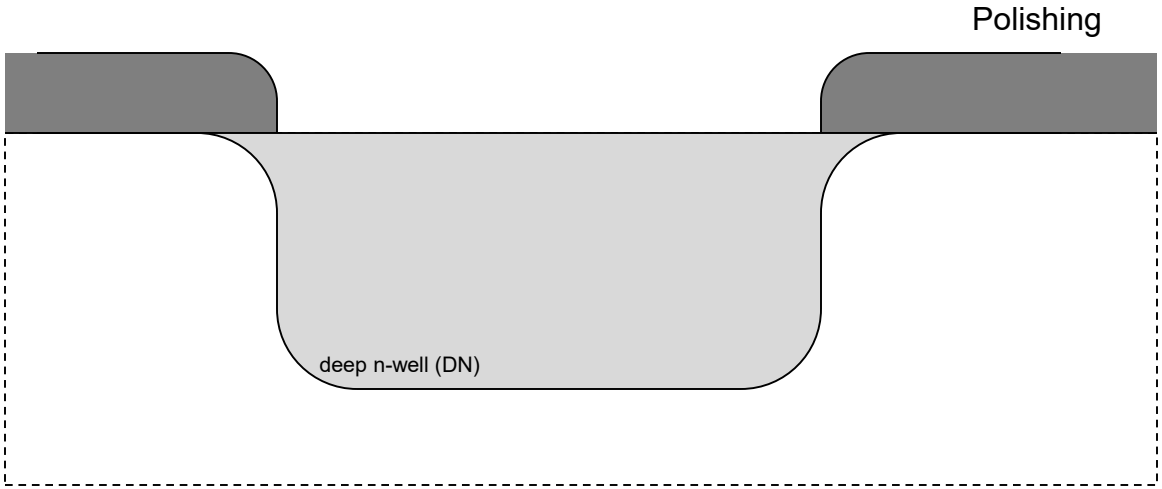


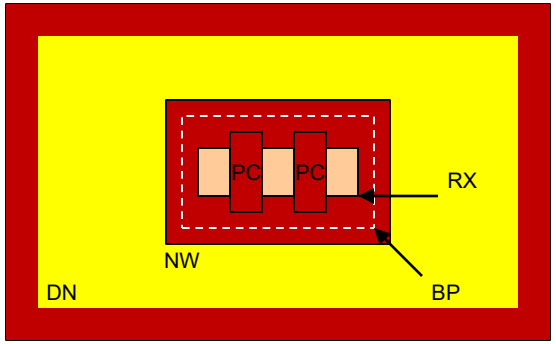

DN
Transparent part
Not transparent
Mask
SiN
PC
PC
RX
NW
DN
BP

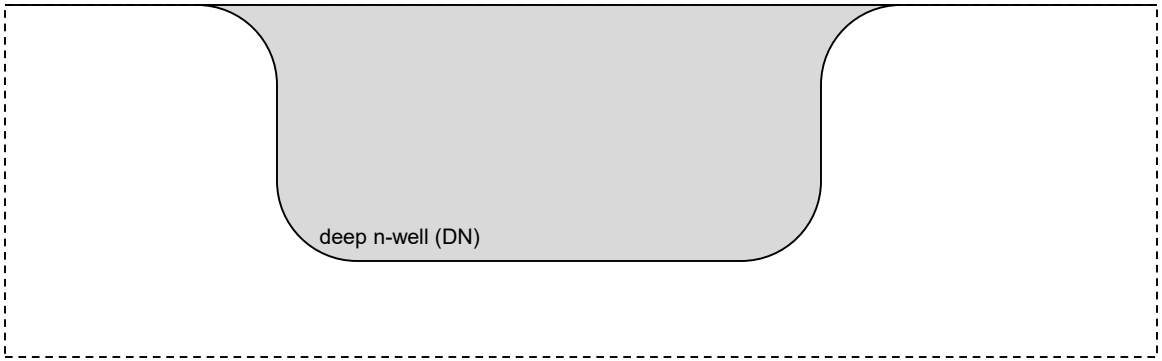

DN
Etching
Mask
(Glass and metal)
Secondary
mask (SiN)
PC
PC
RX
NW
DN
BP

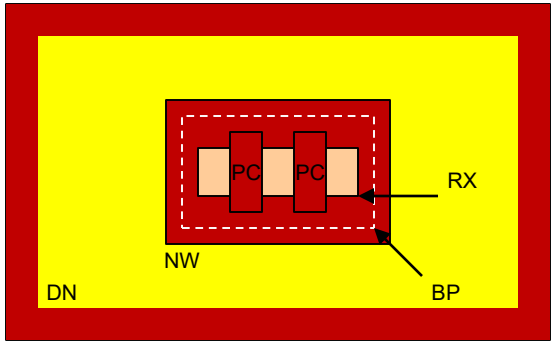

Ion implantation or diffusion
deep n-well (DN)

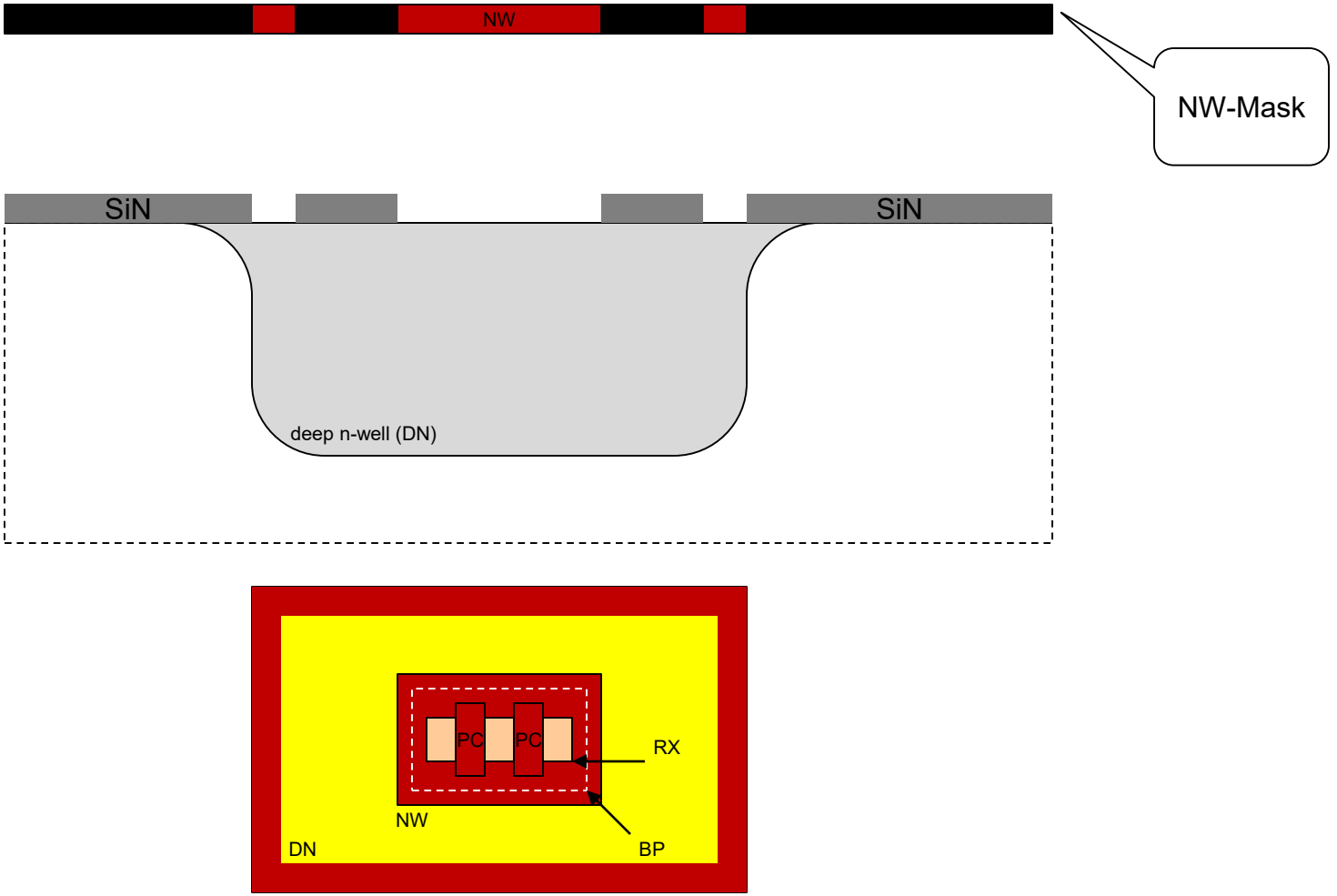

PC
PC
RX
NW
DN
BP

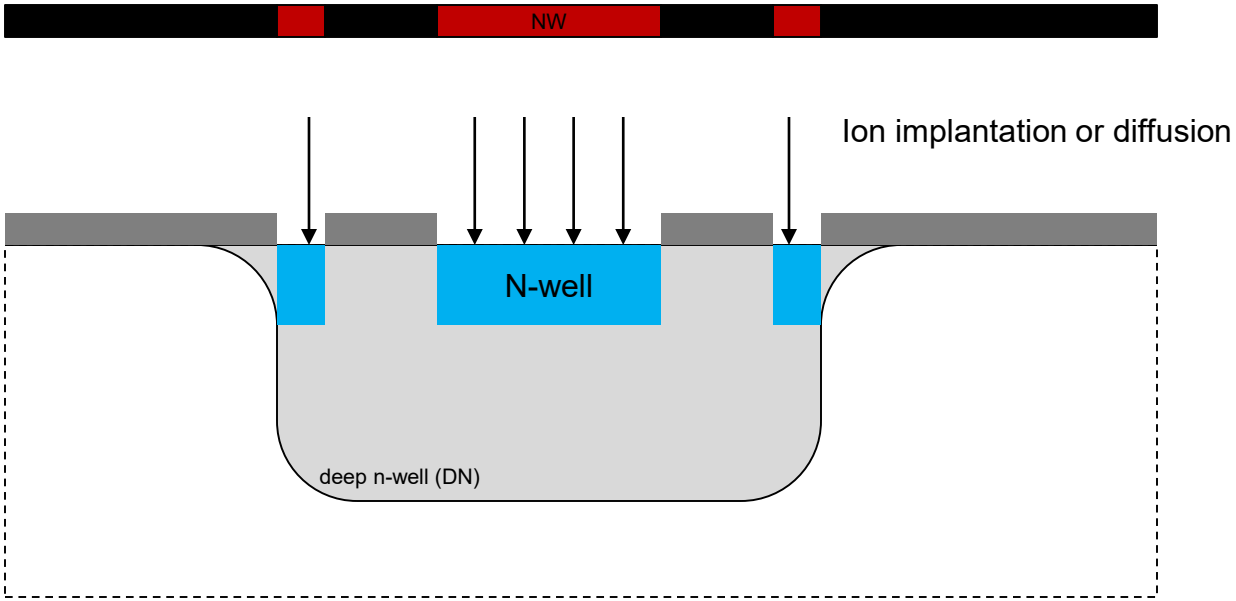

Polishing
deep n-well (DN)

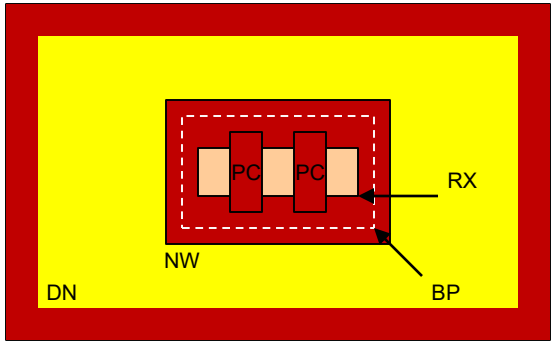

PC
PC
RX
NW
DN
BP

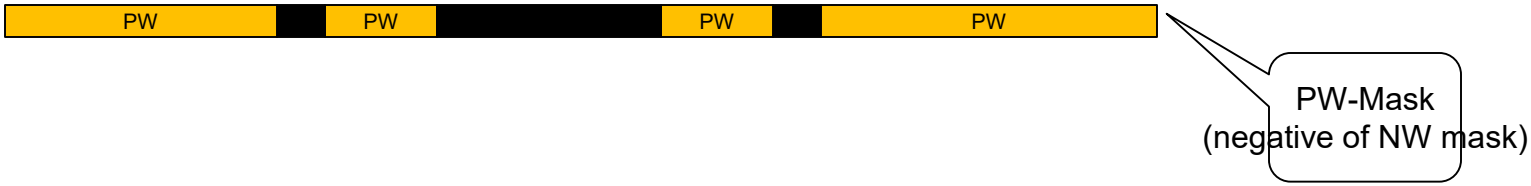

deep n-well (DN)

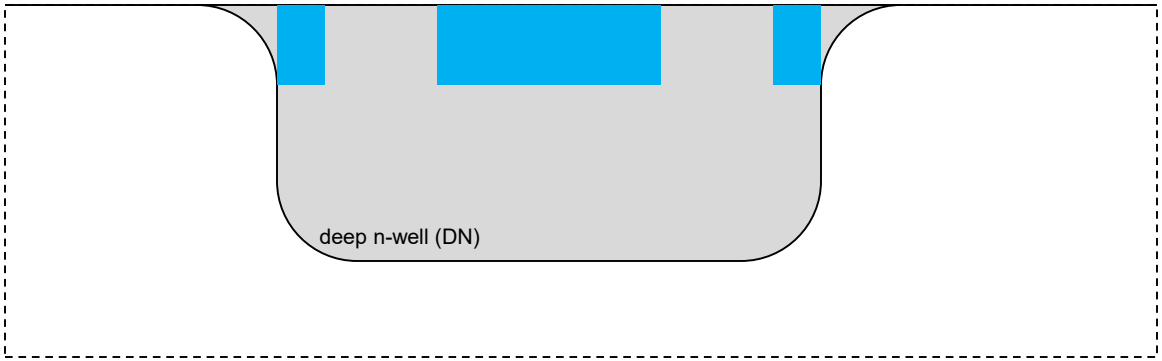

PC
PC
RX
NW
DN
BP

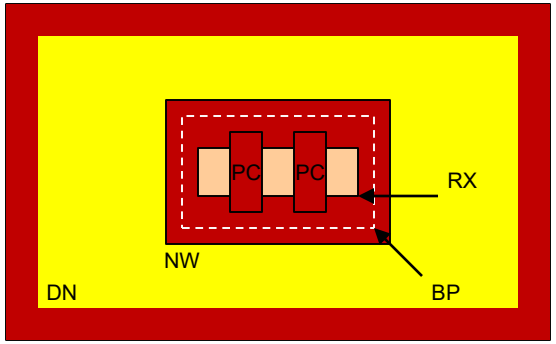

NW
NW-Mask
SiN
SiN
deep n-well (DN)
PC
PC
RX
NW
DN
BP

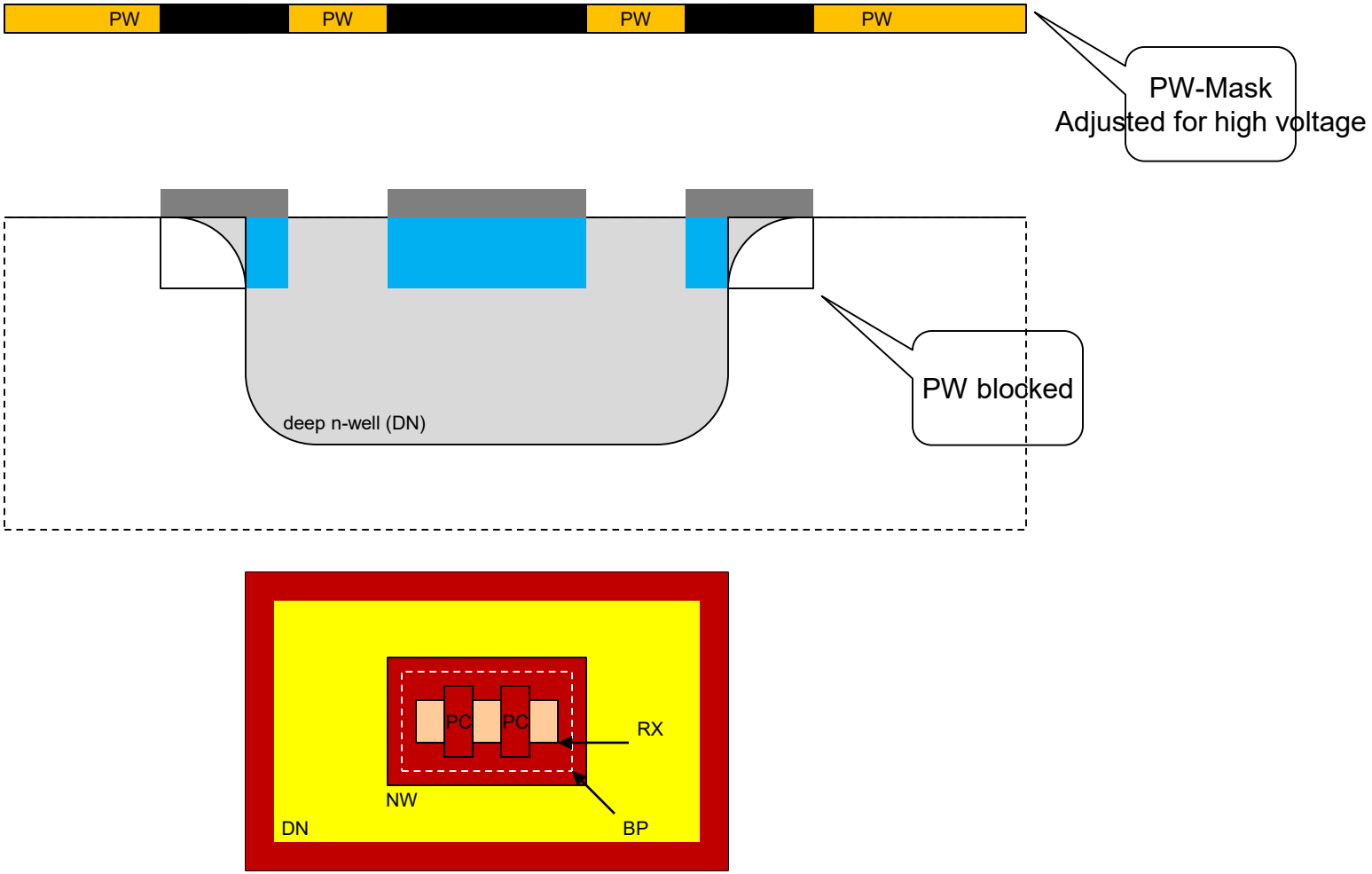

NW
Ion implantation or diffusion
N-well
deep n-well (DN)

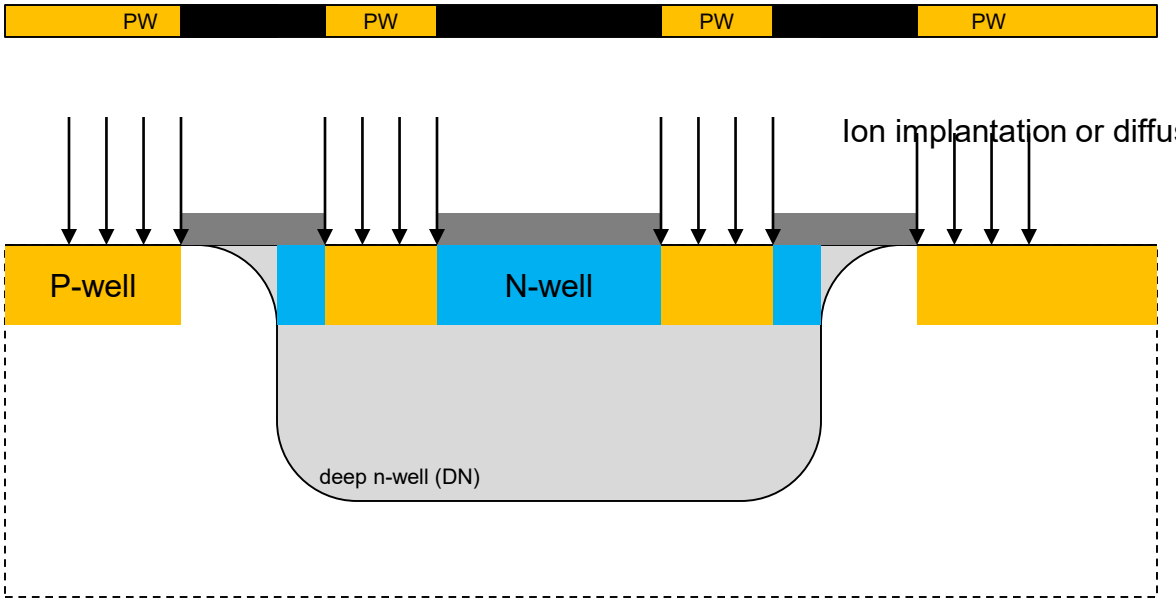

PC
PC
RX
NW
DN
BP

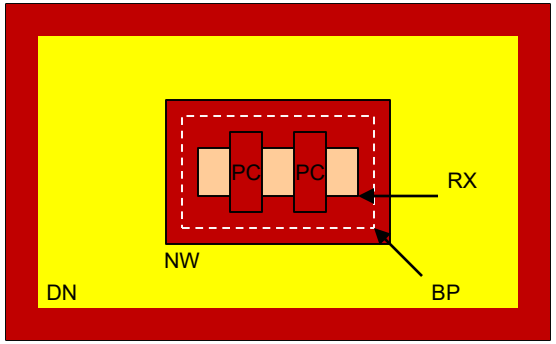

PW
PW
PW
PW
PW-Mask
(negative of NW mask)

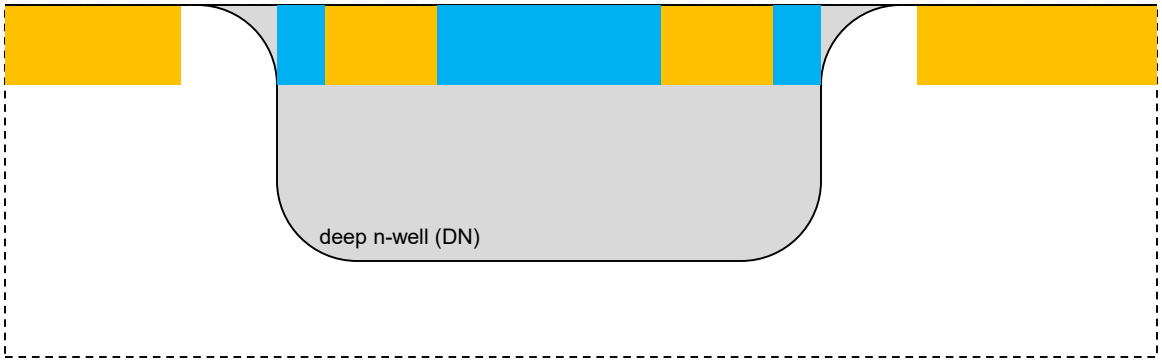

deep n-well (DN)

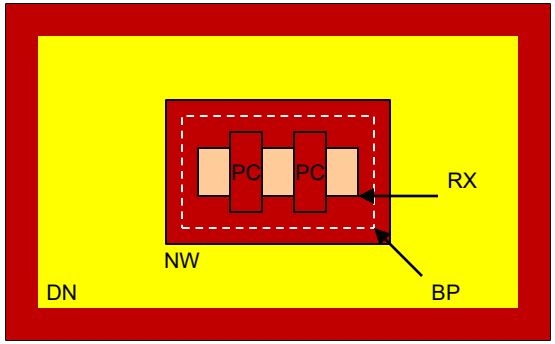

PC
PC
RX
NW
DN
BP

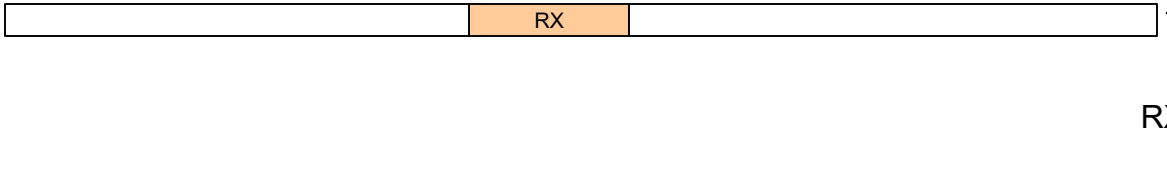

PW
PW
PW
PW
PW-Mask
Adjusted for high voltage
deep n-well (DN)
PW blocked
PC
PC
RX
NW
DN
BP

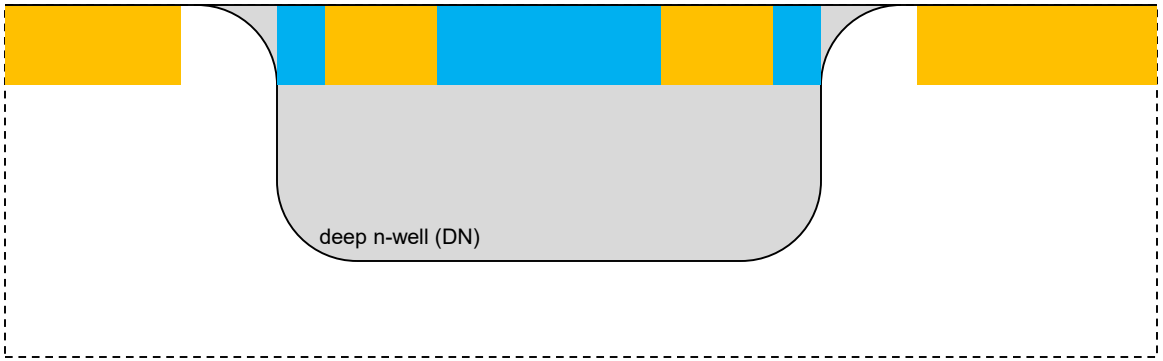

PW
PW
PW
PW
Ion implantation or diffusion
P-well
N-well
deep n-well (DN)

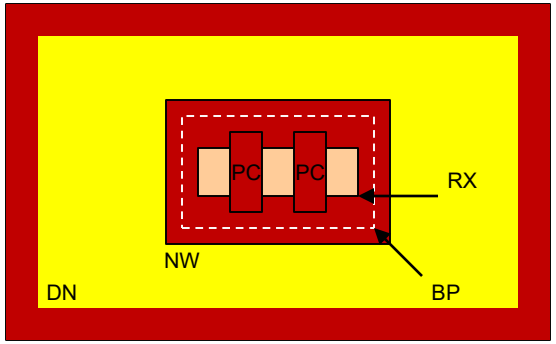

PC
PC
RX
NW
DN
BP


deep n-well (DN)

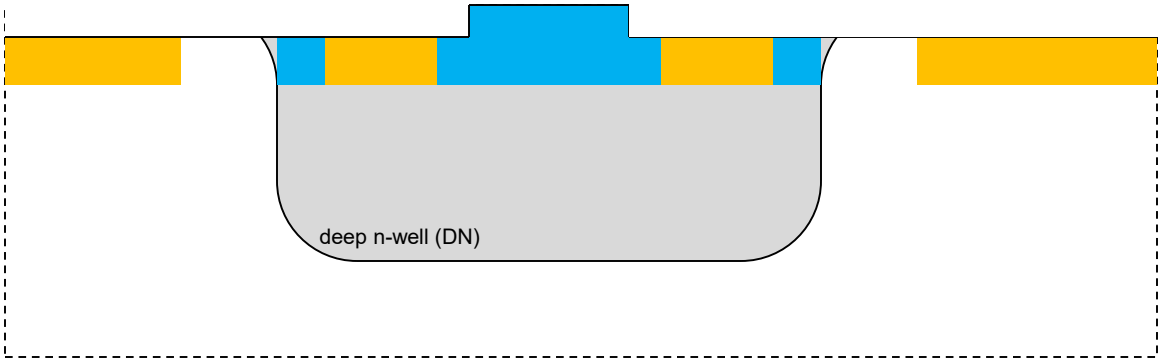

PC
PC
RX
NW
DN
BP

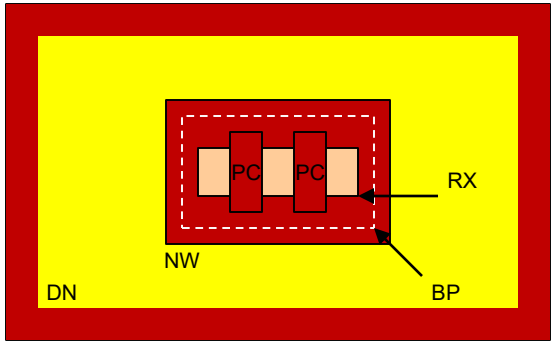

RX
RX-Mask defines active regions


deep n-well (DN)

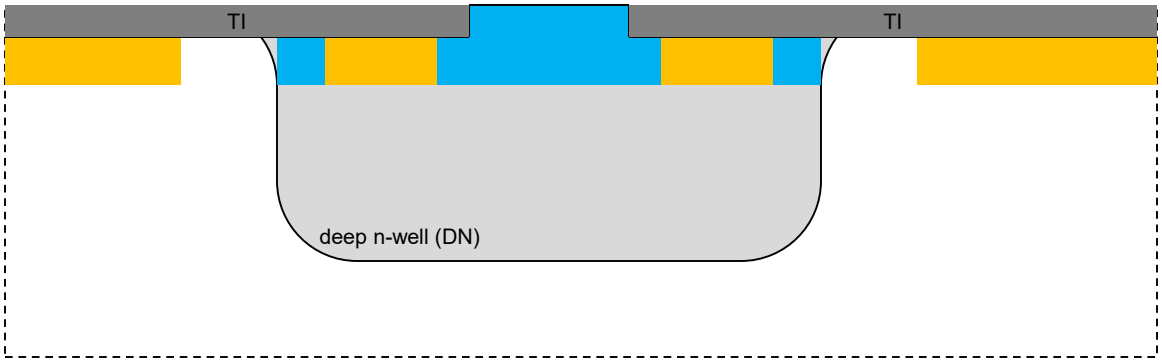

PC
PC
RX
NW
DN
BP

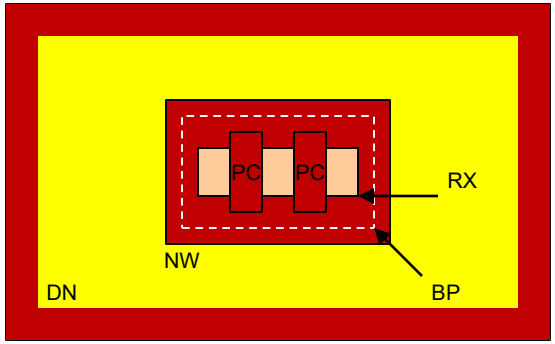
Etching of a trench



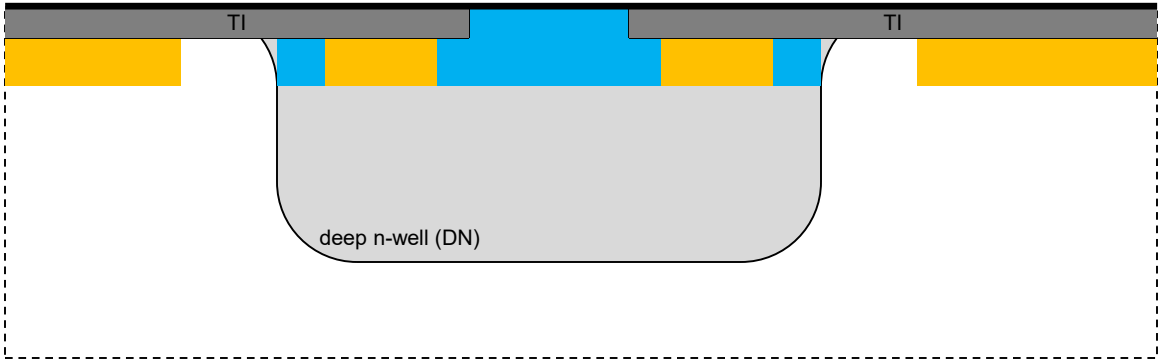


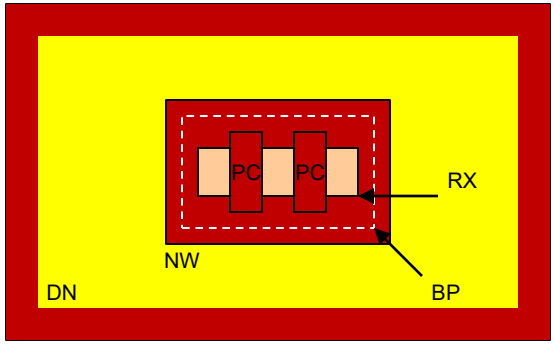
Trench filled with oxide (trench isolation)

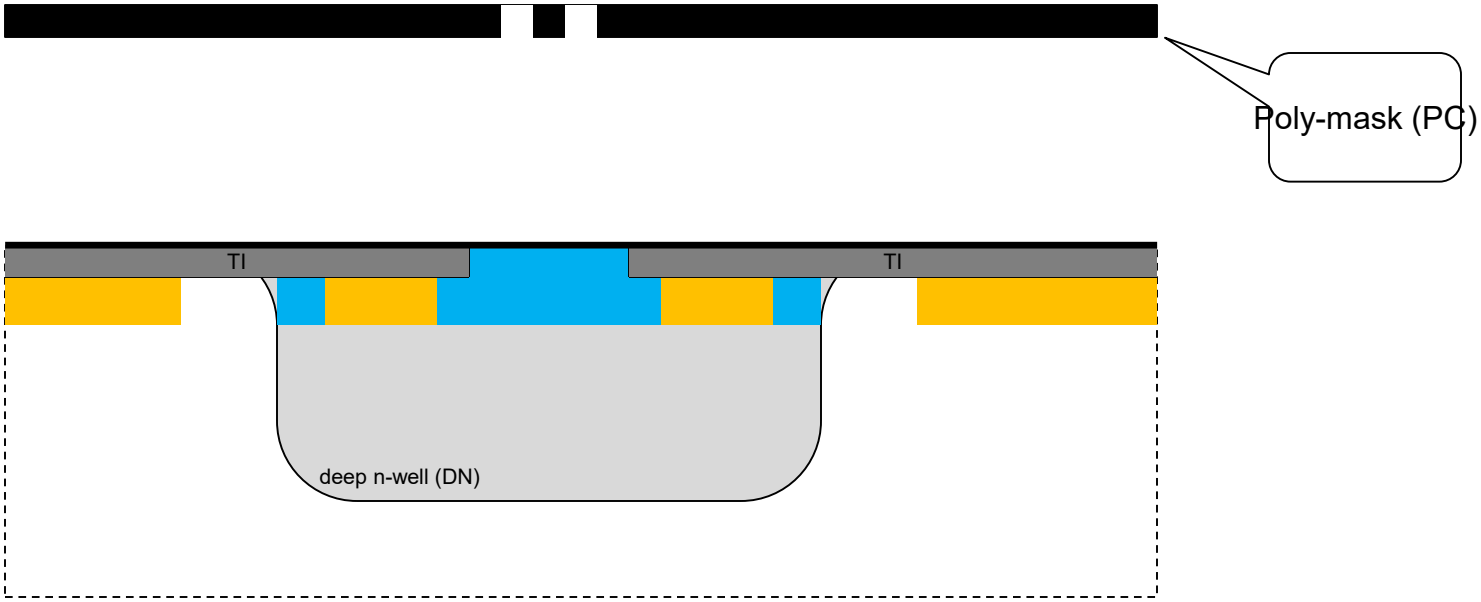




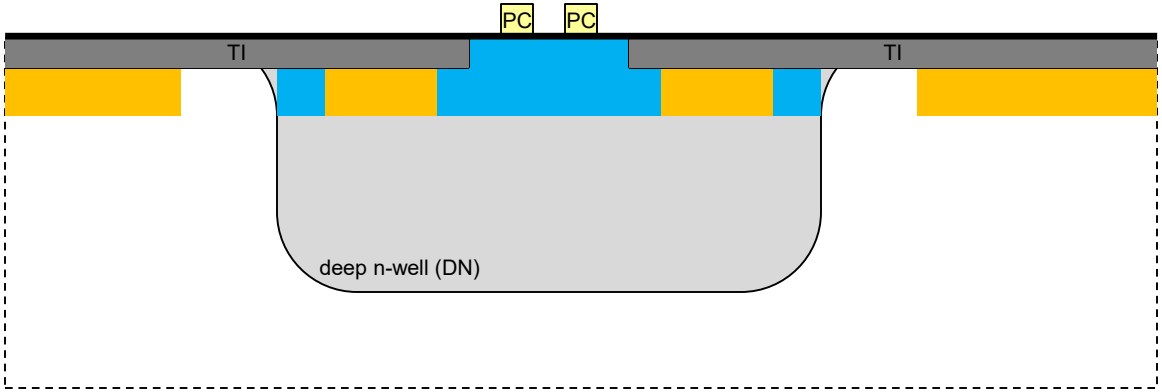
Gate oxide is formed by thermal oxidation

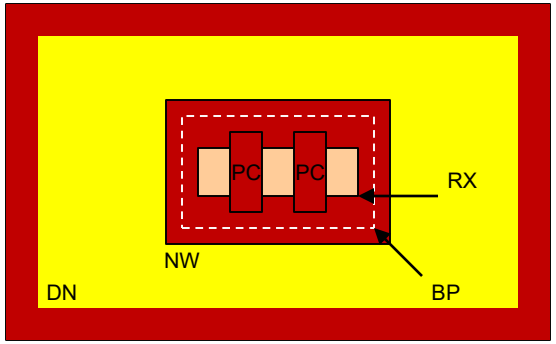


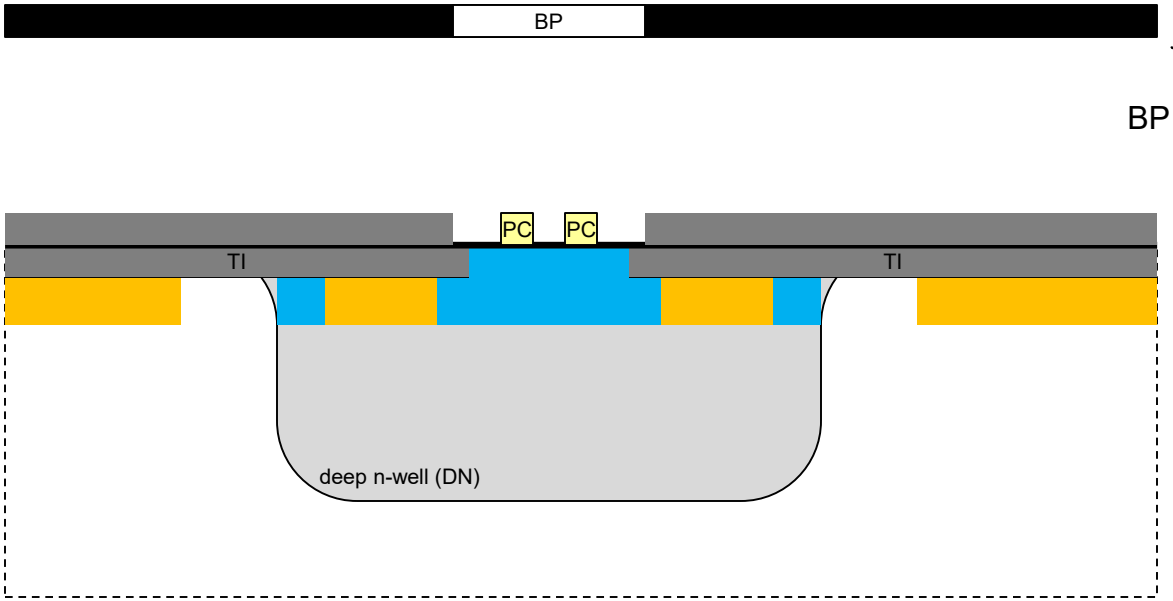


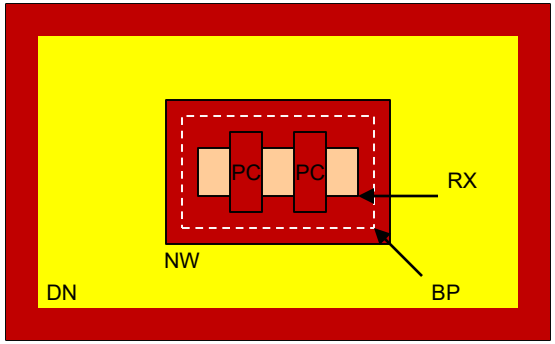

Poly-mask (PC)
TI
TI
deep n-well (DN)
PC
PC
RX
NW
DN
BP

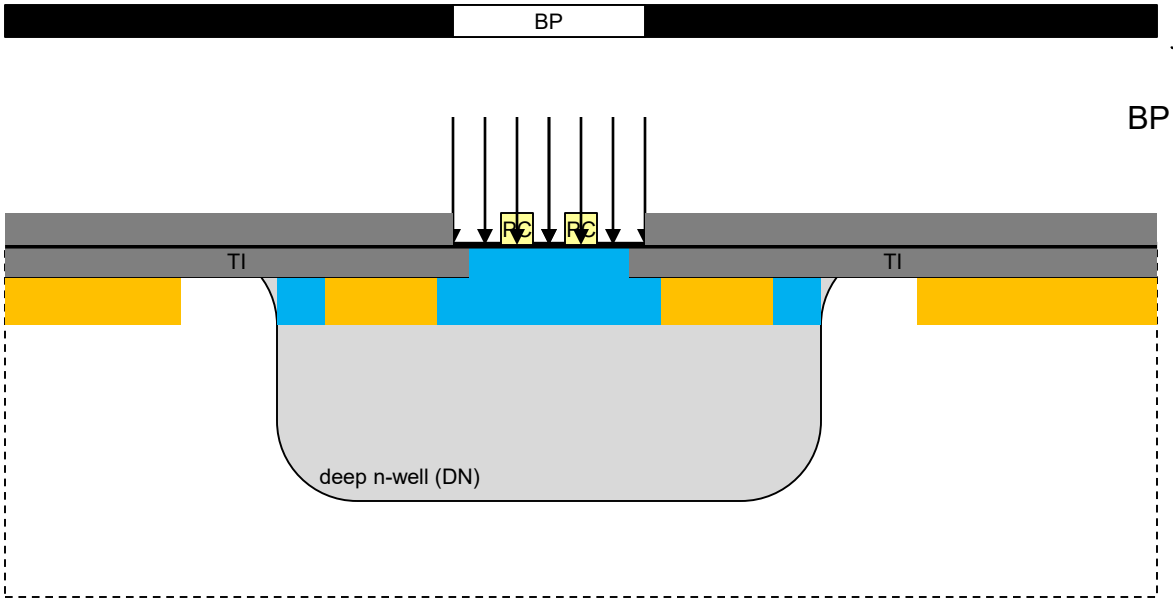
Polysilicon-contacts (PC) formed by deposition

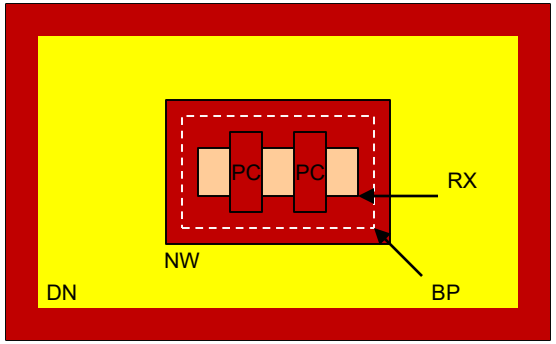


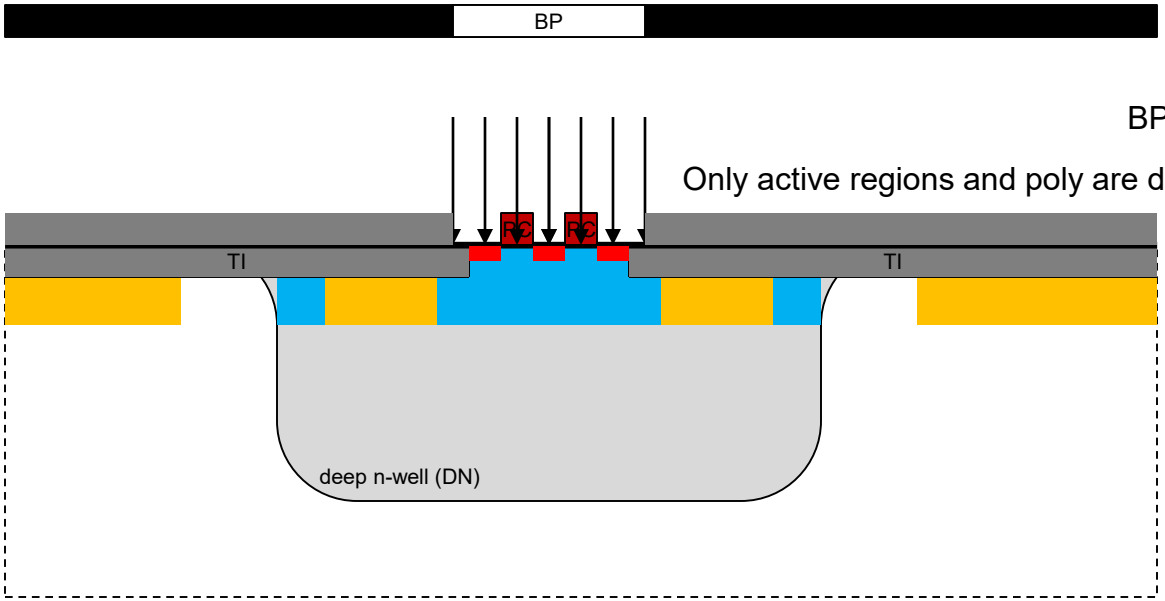


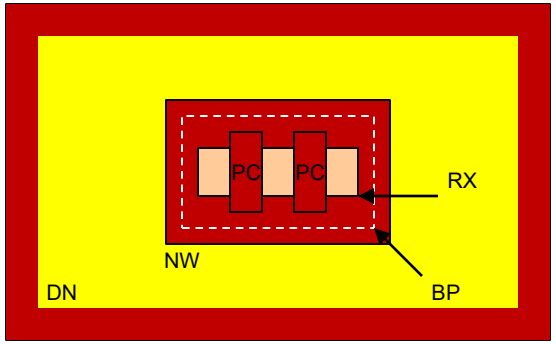

BP
BP mask defines p+ doped layers
PC
PC
TI
TI
deep n-well (DN)

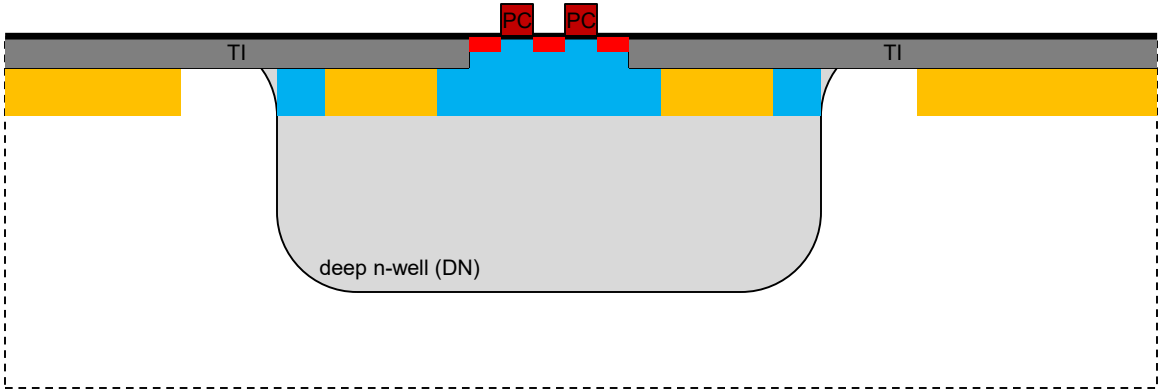

PC
PC
RX
NW
DN
BP

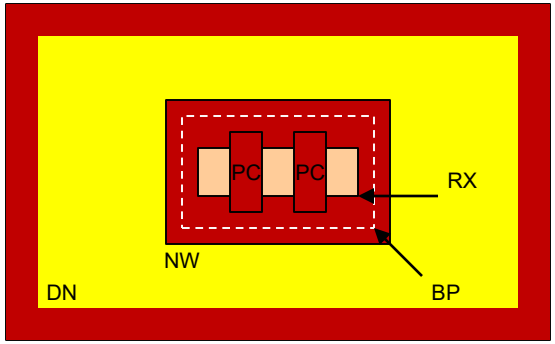

BP
BP mask defines p+ doped layers
PC
PC
TI
TI
deep n-well (DN)


PC
PC
RX
NW
DN
BP


BP
BP mask defines p+ doped layers
Only active regions and poly are doped
RX
RX
TI
TI
deep n-well (DN)


PC
PC
RX
NW
DN
BP


PC
PC
TI
TI
deep n-well (DN)


PC
PC
RX
NW
DN
BP